N32G032x Series Errata Sheet V1.2.0

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1 Errata List

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2 PWR

2.1 Power on after power off

Description

When the power supply is powered off, the power is not completely powered down to about 1.6V and then powered on to the normal working voltage, the power-on may not be successful.

Resolution

When the MCU is powered off, it is necessary to ensure that the chip VDD voltage drops below 100mV, and then power on to the normal operating voltage.

2.2 STOP+ mode

Description

Version A/B supports the STOP+ mode, while Version C has removed the STOP+ mode to address the rare issue of power-on failure caused by IO reverse current leakage prior to VDD power-on.

Solution

When configuring the STOP mode, the STOPPLUSEN bit should be disabled, and the PDSTOP bit should be selected to enter the STOP mode. There may be minor changes in power consumption (STOP power consumption meets the specified parameters in the data manual).

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3 RCC

3.1 When running the program, the LSI is biased

Description

When the LSI is running the program, the Jitter is large, the average frequency (1S time) is 30K±1KHz, and the instantaneous frequency is 20K~45KHz.

Resolution

For precise timing, it is recommended that customers use LSE instead of LSI.

3.2 LSE is affected by toggling of adjacent pins

Description

LSE is affected by toggling of adjacent pins.

Resolution

Avoid toggling of adjacent pins of LSE

3.3 Abnormal functionality after PLL division reset

Description

Abnormal functionality after PLL division reset.

Resolution

After a system reset, configure the PLL output division value to 01 first, and then configure it to 00 to reset the functionality.

3.4 HSI output fluctuations

Description

HSI output fluctuations, with periodic jitter frequency of 2MHz on V_{DDD}, resulting in HSI frequency deviation of approximately ±8%.

Resolution

None

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3.5 LSE has difficulty starting at high temperatures of 105 ℃

Description

LSE has difficulty starting at high temperatures of 105 ℃.

Resolution

None

3.6 LSE Power-up/down related issue

Description

If LSE (Low-Speed External) oscillator is enabled and the MCU is not fully powered down to around 1.6V before being powered up to normal operating voltage, there might be difficulties in successful power-up.

Resolution

If LSE has been enabled and the MCU is powered down, ensure that the chip's VDD voltage drops below 100mV before powering up to the normal operating voltage.

3.7 HSE instability causes chips to run off

Description

When enabling HSE and waiting for the HSE ready flag to be set to run the code directly, the system program may be unstably due to the HSE clock, causing the program to run away.

Resolution

After enabling HSE, add a software delay of about 10 milliseconds, then wait for the HSE Ready flag to be set before running the code.

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4 GPIO and AFIO

4.1 GPIO analog function

Description

When the 4 GPIOs PA1/PA2/PA3/PA4 are in the high-level output state, when they switch to the analog function, there will be a short output voltage drop of about 30mv during the switching process.

Resolution

Avoid the above methods of use.

4.2 IO reverse current

Description

If the IO that does not support failsafe is powered on before VDD, an exception may occur at this time, and the external pin reset cannot return to normal after the exception.

Resolution

It is recommended that customers use the power-on of VDD prior to the power-on of IO.

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5 ADC

5.1 When the injection channel is triggered, the regular channel is also triggered

Description

The ADC converts continuously, and the external trigger of the regular channel is disabled. When the software or hardware trigger injection channel conversion, the regular channel may be converted, and the corresponding status bit of the regular channel conversion will be set.

Resolution

Ignore the status bit and data generated by the regular channel.

5.2 ADC injected channel conversion

Description

Injecting channel conversion triggered at the moment when regular channel conversion is completed, the injected channel conversion cannot be completed.

Resolution

None

5.3 ADC input noise

Description

When there's high-frequency noise around 10MHz in the ADC input signal, the ADC may exhibit anomalies approaching the saturation value of 4096.

Resolution

None

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5.4 Read ADC data register ADC_DAT (ADC_JDATx) value exception issue after the ADC ENDC (or JENDC) flag is set

Description

When the regular sequence conversion completion flag ENDC (injection sequence conversion completion flag JENDC) is set, the ADC Data Register ADC_DAT (ADC_JDATx) is read immediately, possibly with the result of the previous conversion.

Resolution

1. When the ENDC/JENDC flag is set, delay 8 ADC_CLK clocks before reading the ADC data registers (ADC_DAT/ADC_JDATx);
2. In some scenarios, use the any regular channel conversion completion flag ENDCA (any injection channel conversion completion flag JENDCA) flag instead of the ENDC (JENDCA) flag.

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6 OPAMP

6.1 The output impedance of OPAMP is higher than expected.

Description

The output impedance of the operational amplifier (OPAMP) is higher than expected.

Resolution

None

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7 SPI&I2S

7.1 SPI

7.1.1 SPI baud rate setting when CRC is enabled

Description

When the CRC check function is turned on, depending on the working environment of the SPI interface, such as board-level delay, ambient temperature, etc., both the SPI master and slave will have CRC check exceptions.

In the ideal room temperature environment of the laboratory, when the SPI clock is greater than 12MHz, an abnormal CRC check error may occur.

Resolution

When the CRC function is enabled, it is recommended that the CRC clock frequency configuration should not exceed 12MHz.

When a CRC exception error occurs, reduce the SPI baud rate configuration.

7.1.2 Slave mode CRC check

Description

SPI works in slave mode and CRC check has been enabled, even if the NSS pin is high level, as long as the SPI receives the clock signal, the CRC calculation will still be performed

Resolution

Before using the CRC check, clear the CRC data register so that the CRC check of the master and slave devices can be synchronized

The steps to clear are as follows：

1. SPI enable bit reset (set 0)
2. CRC check bit reset (set 0)
3. CRC check bit set (set 1)
4. SPI enable bit set (set 1)

7.1.3 When the power supply is 1.8V~2.0V, the SPI data rate may not reach 12Mbps

Description

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When the power supply is 1.8V~2.0V, the SPI data rate may not reach 12Mbps depending on the IO and board-level wiring delay characteristics.

The highest communication rate measured in the ideal environment of the laboratory is 12M:

Resolution

If customers have 1.8V high temperature and low temperature SPI communication requirements, it is recommended to contact Nationstech Company for technical support.

7.2 I2S

7.2.1 PCM long frame mode

Description

When I2S works in master mode, PCM long frame mode, and the data format is "32bit" or "16bit extended to 32bit", the WS signal is one cycle per 16bit instead of 32bit.

Resolution

When I2S is the master mode and the long frame mode must be used, the 16bit data mode should be used.

7.2.2 No MCLK output in I2S master mode

Description

When the I2S is operating in master mode with the MCLK enable option turned on, and I2S transmission starts, there is no output of the MCLK signal.

Resolution

None

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8 I2C

8.1 A software event that must be managed before the current byte is transferred.

Description

When EV7, EV7_1, EV6_1, EV6, EV2, EV8, and EV3 events occur, the events must be processed before the current byte is transferred, otherwise there may be a problem of reading an extra byte, reading duplicate data, or losing data. If the software does not read the N-1th byte before the stop signal is generated, the Nth byte in the shift register is corrupted (shifted one bit to the left).

Resolution

1. When using I2C to transfer more than one byte, try to use DMA mode
2. When using I2C interrupt, adjust the interrupt priority to the highest priority of the application
3. When the read data reaches the N-1th byte:
   a) Detect BSF as 1
   b) Configure SCL as GPIO open-drain output and set it to 0
   c) Set STOPGEN as 1
   d) Read the N-1th byte
   e) Configure SCL as I2C multiplexing function open-drain output mode
   f) read the last byte

8.2 Attentions when reading a single byte at time

Description

In the master read mode, when the length of the read byte is a single byte, a read data error may occur.

Resolution

When read single byte：

a) After receive ADDRF
b) Set ACKEN bit as 0
c) Clear ADDRF bit（Cleared by reading STS1 and then STS2）
d) Set STOPGEN as 1
e) Read last byte。

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8.3 Using DMA simultaneously with other peripherals

Description

While using DMA for I2C communication, if other peripherals are also using DMA, it can lead to abnormal I2C communication.

Resolution

1, Disable DMA for other peripherals while using DMA for I2C communication.

2, Set the DMALAST bit in I2C->CTRL2 when receiving the second-to-last byte of data.

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9 USART

9.1 Parity error flag

Description

During the reception of one byte of data, before the stop bit is received, a parity error is detected, and the parity error flag is set. During this period, the parity error flag cannot be cleared by software (reading the status register and then reading the data register). If the parity error interrupt is enabled, the parity error interrupt handler will be entered multiple times.

Resolution

After the read data buffer flag is set, after receiving the data, the operation of clearing the parity error flag is performed. If the parity error interrupt is enabled, in order to avoid entering the interrupt processing function multiple times, when the parity error interrupt is entered for the first time, the parity error interrupt is turned off, and after the data is received, the parity error interrupt is turned on again.

9.2 RTS hardware flow control

Description

Enable RTS hardware flow control. When the USART receives data, the RTS signal will be automatically pulled high. If the byte data is not read from the data register in time, and a new byte is sent to the USART (violating the flow control protocol), the RTS signal will be pulled low again. USART waits again to receive the next frame of data.

Resolution

Before the next new data is received, the data is read out from the data register in time.

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10 TIM

10.1 TIM overcapture

Description

When reading the capture data register data (under normal circumstances, the read data register operation will cause the capture flag to be cleared), a trigger capture is generated externally, even if the previous capture has been correctly read and the new capture data is also is sent to the register exactly, but the overcapture flag is still detected. The system is critical for overcapture, but no capture data is lost.

Resolution

None

10.2 ADTIM and GPTIM cannot generate compare events under certain circumstances

Description

In edge-aligned mode, in up-counting PWM1 mode, when the current PWM cycle CCDATx shadow register >= AR value, the shadow register value of CCDATx in the next PWM cycle is 0. At the moment when the PWM cycle counter is 0, although the counter value = CCDATx shadow register value = 0 and OCxREF = 0, but still no compare event is generated.

Resolution

If it is not required that "the compare event is generated at the time when the counter value = CCDATx shadow register value =0", the compare event generated through another channel can replace the compare event that is not generated.

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11 LPTIM

11.1 LPTIM COUNTMODE counting

Description

When configuring the LPTIM with the clock source set to internal clock source, and the counter mode set so that the counter increments with every valid clock pulse on LPTIM external Input1, the counter value (CNT) can only count up to ARR-1. Other configurations can count up to ARR.

Resolution

None

11.2 LPTIM triggering only "compare match interrupt"

Description

The LPTIM can only trigger "compare match interrupt."

Resolution

None

11.3 LPTIM ARROK and CMPOK interrupt sources limited functionality

Description

ARROK and CMPOK interrupt sources have limited functionality: they can only generate interrupts when PRE_LOAD_MODE = 1.

Resolution

When PRE_LOAD_MODE = 0, it is recommended to configure the ARR and CMP registers before enabling LPTIM.

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12 RTC

12.1 RTC timing

Description

While the RTC is operating, both external reset and system reset will cause the clocks (HSE, LSE, LSI) provided to the RTC to pause, leading to a pause in RTC counting.

Resolution

None

12.2 RTC subsecond match

Description

The RTC programmable alarm clock function does not enable matching of date, hour, minute and second, but only enables matching of sub-seconds (that is, an alarm interrupt is generated when sub-seconds match in every second). The alarm interrupt cannot be generated in the first sub-second match after the alarm function is enabled, and the alarm interrupt is generated for each sub-second match after that.

Resolution

None

12.3 RTC second match

Description

When the alarm clock configuration second matches, the chip enters the SLEEP mode. When the alarm interrupt is generated to wake up the chip from SLEEP, and the interrupt processing function is executed (only the operation of clearing the interrupt flag bit is performed), it immediately enters the STOP mode. The next alarm interrupt cannot wake the chip from STOP mode.

Resolution

Before setting the RTC time, you need to enter the RTC initialization mode. Before entering the RTC initialization mode, you need to wait for the value of the sub-second register to be less than the synchronous prescaler value and cannot be 0.

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12.4 RTC calendar function cannot be initialized multiple times within 1 second

Description

The RTC calendar function is initialized multiple times within 1 second, so that the RTC alarm clock interrupt cannot be generated.

Resolution

The interval between two initializations of the RTC calendar function is more than 1 second.

12.5 RTC mistakenly triggers TISOVF flag bit

Description

When the system wakes up from STANDBY mode, or when the IWDG timeout generates a system reset, the RTC will probabilistically trigger the TISOVF flag bit by mistake.

Workaround

Before entering STANDBY mode or IWDG timeout, When the SHOPF flag is 0, configure the RTC_SCTRL.SUBF[14:0] register, and the flag will be set to 1.When the SHOPF flag is 0 again, configure the RTC_SCTRL.SUBF[14:0] register for the second time; note that the NRST cannot be triggered when the software executes the above process clock.

12.6 RTC_DATE register lock

Description

1. Before the system software reset, the RTC_DATE register is not read after reading the RTC_SUBS or RTC_TSH shadow register, and the RTC_DATE register will restores the default value after the system software resets and initializes the RTC without configuration or reads the RTC_DATE register;

2. When reading the calendar, after reading the RTC_SUBS or RTC_TSH shadow register, the value of the RTC_DATE register remains unchanged;

Resolution

1. Read the RTC_DATE register before initializing the RTC;

2. After reading the RTC_SUBS or RTC_TSH shadow register, read the RTC_DATE register;

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13 CAN

13.1 CAN Active Error

Description

While the CAN is in normal mode, if the CAN bit is hard synchronized and the baud rate deviation of other nodes on the bus is too large (close to or exceeding the synchronization segment), the CAN module is prone to report active errors.

Resolution

None

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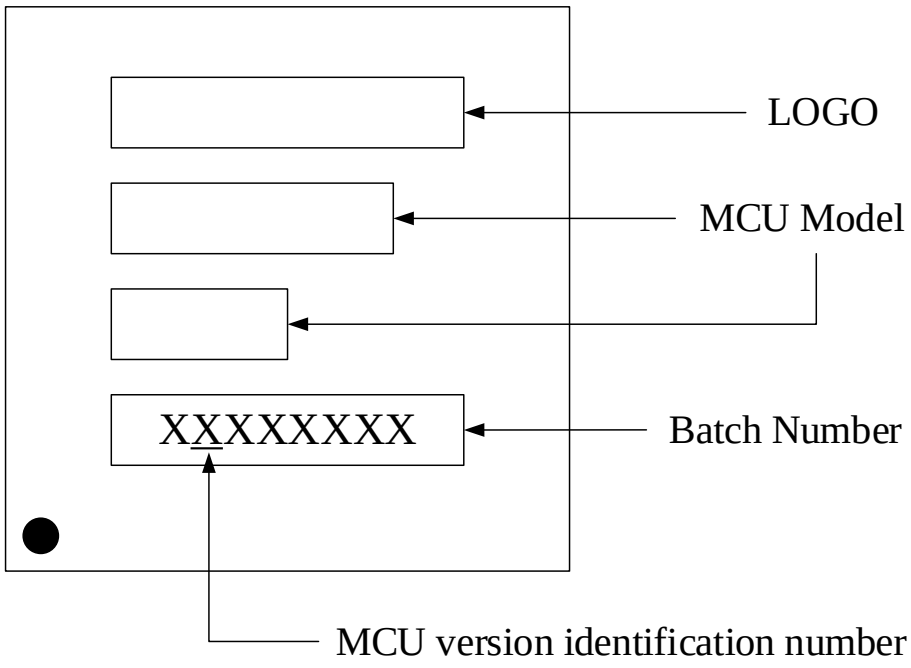
14 Marking information



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15 Version history

Date	Version	Description
2023.8.22	V1.1.0	Initial version
2023.9.19	V1.2.0	1. Add section 2.2 2. Section 7.1.1, modify SPI clock not greater than 14MHz to not greater than 12MHz; 3. Section 7.1.3, modify SPI clock data transfer rate not greater than 18MHz to not greater than 12MHz. 4. Add section 5.4

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