N32G4FRxC/xE Product Brief

N32G4FR series adopts 32 bit ARM Cortex-M4 core, the highest working frequency is 144MHz, supports floating-point operations and DSP instructions, built-in cryptographic algorithm hardware acceleration engine, integrates up to 512KB encrypted Flash memory, 144KB SRAM, can be used to securely store fingerprint information, supports Mainstream semiconductor fingerprint and optical fingerprint sensor, integrated with abundant U(S)ART, I2C, SPI, QSPI, USB, ADC, DAC, SDIO and other general peripheral interfaces

Main features

- **CPU core**
  - 32-bit ARM Cortex-M4 core + FPU, single-cycle hardware multiply and divide instructions, support DSP instructions and MPU
  - Built-in 8KB instruction Cache, support Flash acceleration unit execution program 0 wait
  - Run up to 144MHz, 180DMIPS
- **Memory**
  - Up to 512KByte embedded Flash memory, support encrypted storage, partition management and data protection, support hardware ECC verification, 100,000 erasing times, 10 years data retention
  - 144KByte embedded SRAM (including 16KByte Retention RAM), supporting hardware parity check
- **Low power management**
  - Standby mode: 3uA, 84 backup registers are retained, all IOs are retained, optional RTC Run, 16KByte Retention SRAM retention, support VBAT pin independent power supply, 100us fast wake-up
  - Stop2 mode: 5uA, RTC Run, 16KByte Retention SRAM retention, CPU register retention, all IO retention, 40us fast wake-up
  - Stop0 mode: 120uA, RTC Run, all SRAM retained, all IO retained, 20us fast wake-up
- **Clock**
  - 4MHz~32MHz external high-speed crystal
  - 32.768KHz external low-speed crystal
  - Internal high-speed RC 8MHz
  - Internal low-speed RC 40KHz
  - Built-in high-speed PLL
  - Supports one-way clock output, which can be configured with system clock, HSE, HSI, or PLL frequency division output
- **Reset**
  - Supports power-on/power-down/brown-out/external pin reset

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- Support watchdog reset, software reset

- **Up to 65 GPIOs with multiplexing function. The maximum flip speed is 50MHz. Most GPIO supports 5V voltage resistance.**
- **Communication interface**
  - 7x U(S)ART interfaces with speeds up to 4.5Mbps, including 3x USART interfaces (supporting ISO7816, IrDA, LIN) and 4x UART interfaces
  - 3x SPI interfaces with speeds up to 36MHz, two of which support I2S
  - 1x QSPI interface with speeds up to 144Mbps
  - 4x I2C interfaces with speeds up to 1MHz, which can be configured in master/slave mode and support dual address response in slave mode
  - 1x USB2.0 Full Speed Device port
  - 2x CAN 2.0B bus interfaces
  - 1x SDIO interface, supporting SD/MMC format
  - 1x DVP (Digital Video Port)
- **High-performance analog interface**
  - 2x 12bit 5Msps high-speed ADCs, available in 12/10/8/6 bit mode, sampling rate up to 9Msps in 6bit mode and up to 16 external single-ended input channels, supporting differential mode
  - 2x 12bit DAC, sampling rate 1Msps
  - Support external input independent reference voltage source
  - All analog interfaces support full voltage from 1.8 to 3.6V
- **2x high-speed DMA controllers, each controller supports 8 channels, channel source address and destination address can be arbitrarily configurable**
- **RTC real-time clock, support leap year perpetual calendar, alarm clock event, periodic wake up, support internal and external clock calibration**
- **Timing counter**
  - 2x 16bit advanced timer counters, support input capture, complementary output, orthogonal coding input and other functions, the highest control accuracy of 6.9ns;Each timer has four independent channels, three of which support 6 complementary PWM output
  - 4x 16bit general timer counters, each timer has four independent channels, support input capture/output comparison /PWM output
  - 2x 16bit basic timer counters
  - 1x 24bit SysTick

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- 1x 7bit Window Watchdog (WWDG)
- 1x 12bit Independent Watchdog (IWDG)

- **Programming mode**
  - Support SWD/JTAG online debugging interface
  - Support UART and USB Bootloader
- **Security features**
  - Built-in cryptographic algorithm hardware acceleration engine
  - Supports AES, DES, SHA, SM1, SM3, SM4, SM7, and MD5 algorithms
  - Flash Storage encryption, Multi-user Partition Management (MMU)
  - TRNG true random number generator
  - CRC16/32 operation
  - Support write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
  - Support security startup, program encryption download, security updates
  - Support clock failure detection, anti-disassembly detection
- **96-bit UID and 128-bit UCID**
- **Working conditions**
  - Operating voltage range: 1.8V~3.6V
  - Operating temperature range: -40℃ ~ 105℃
  - ESD: ±4KV (HBM model), ±1KV (CDM model)
- **Package**
  - QFN32(4mm x 4mm)
  - QFN40(5mm x 5mm)
  - LQFP64(10mm x 10mm)
  - LQFP80(12mm x 12mm)

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1 Ordering information

Figure 1-1 N32G4FR Series Part Number Information

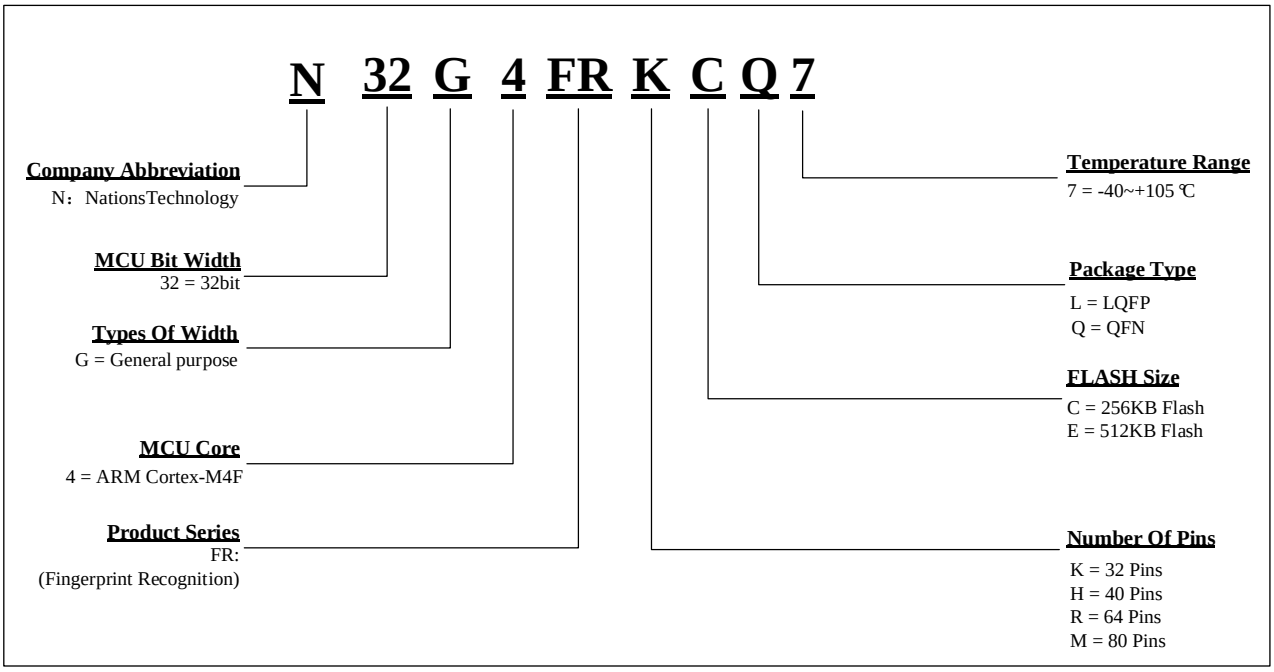

Table 1-1 N32G4FR Series Ordering Code

Ordering code (1)	Package	Package size	Packaging (2)	SPQ(3)	Temperature range
N32G4FRKCQ7	QFN32	4mm*4mm	Tray	490	-40℃ ~ 105℃
N32G4FRKEQ7	QFN32	4mm*4mm	Tray	490	-40℃ ~ 105℃
N32G4FRHCQ7	QFN40	5mm*5mm	Tray	490	-40℃ ~ 105℃
N32G4FRHEQ7	QFN40	5mm*5mm	Tray	490	-40℃ ~ 105℃
N32G4FRREL7	LQFP64	10mm*10mm	Tray	160	-40℃ ~ 105℃
N32G4FRMEL7	LQFP80	12mm*12mm	Tray	119	-40℃ ~ 105℃

1. For the latest detailed ordering information, please refer to the Selection Guide.
2. The packaging provided is the basic packaging. If user has any other requirements, please contact Nations.
3. Minimum packaging quantity.

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2 Product Model Resource configuration

Device type		N32G4FRKC/E		N32G4FRHC/E		N32G4FRRE	N32G4FRME
Flash size（KB）		256	512	256	512	512	512
SRAM size（KB）		144	144	144	144	144	144
CPU frequency		ARM Cortex-M4 @144MHz,180DMIPS					
Work environment		1.8~3.6V/-40~105℃					
Timer	General	4					
	Advanced	2					
	Basic	2					
Communication Interface	SPI	2		3			
	I2S	1		2			
	QSPI	1					
	I2C	3				4	
	USART	1		2		3	
	UART	3		4			
	USB	1					
	CAN	1		2			
	SDIO	No				1	
	DVP	No		1			
GPIO		24		32		51	65
DMA		2					
Number of Channels		16Channel					
12bit ADC		2		2		2	2
Number of channels		7Channel		11Channel		16Channel	16Channel
12bit DAC		2					
Number of channels		2Channel					
Algorithm support		DES/3DES、AES、 SHA1/SHA224/SHA256、SM1、SM3、SM4、SM7、MD5、CRC16/CRC32、TRNG					
Security protection		Read/write protection（RDP/WRP）, storage encryption, partition protection, secure startup					
Package		QFN32		QFN40		LQFP64	LQFP80

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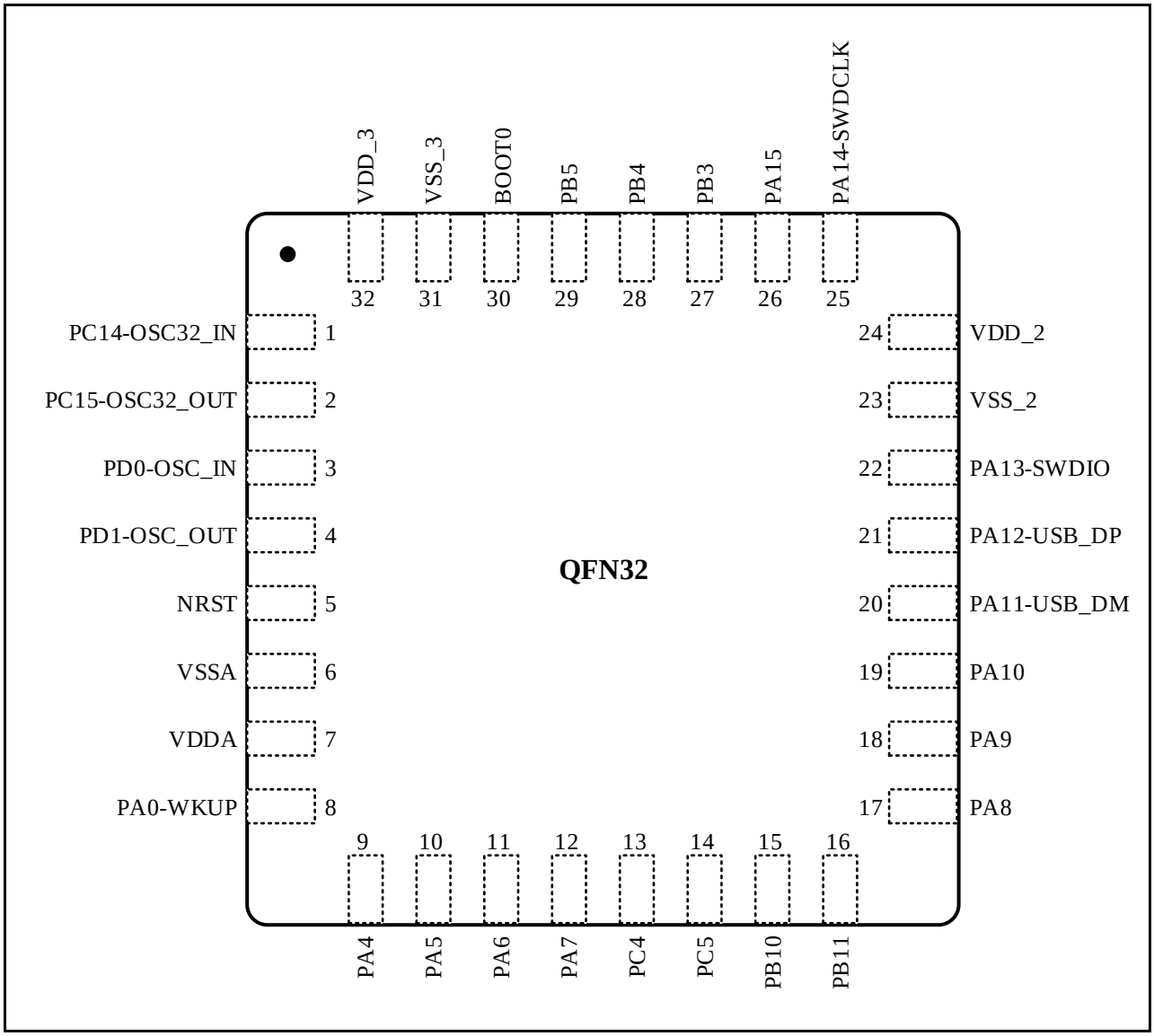
3 Package

3.1 QFN32 package

3.1.1 QFN32 pin distribution



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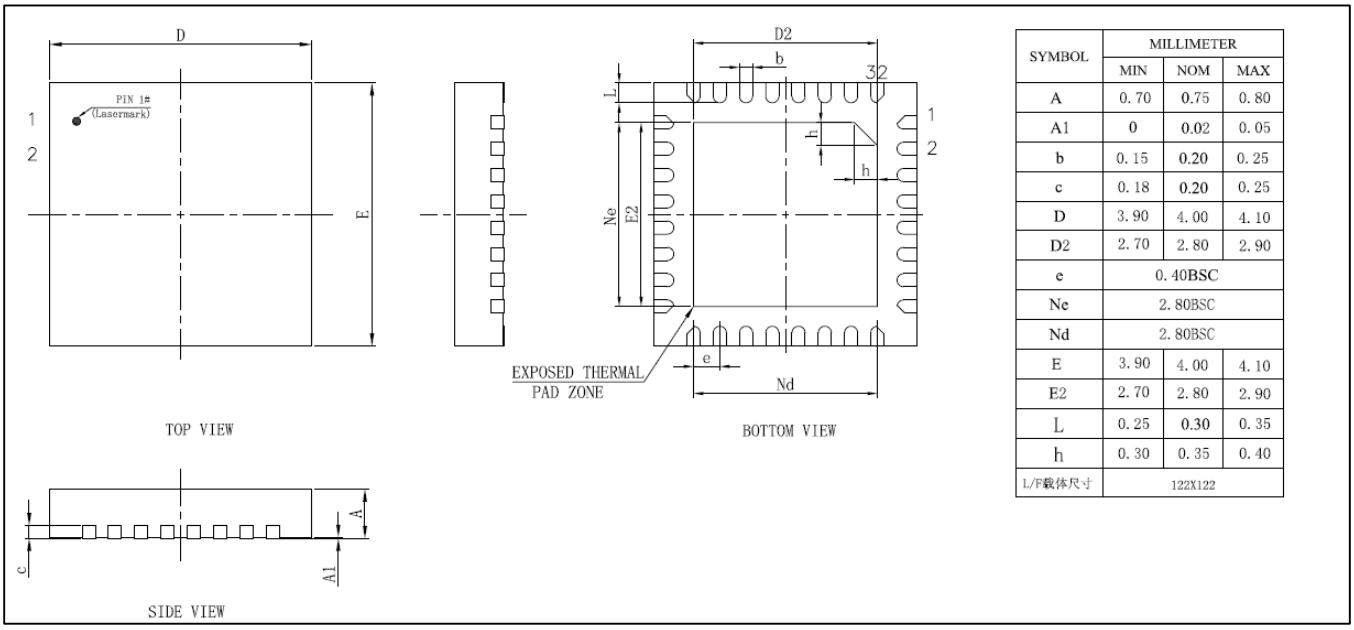
3.1.2 QFN32 package size



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40
L/F载体尺寸	122X122		

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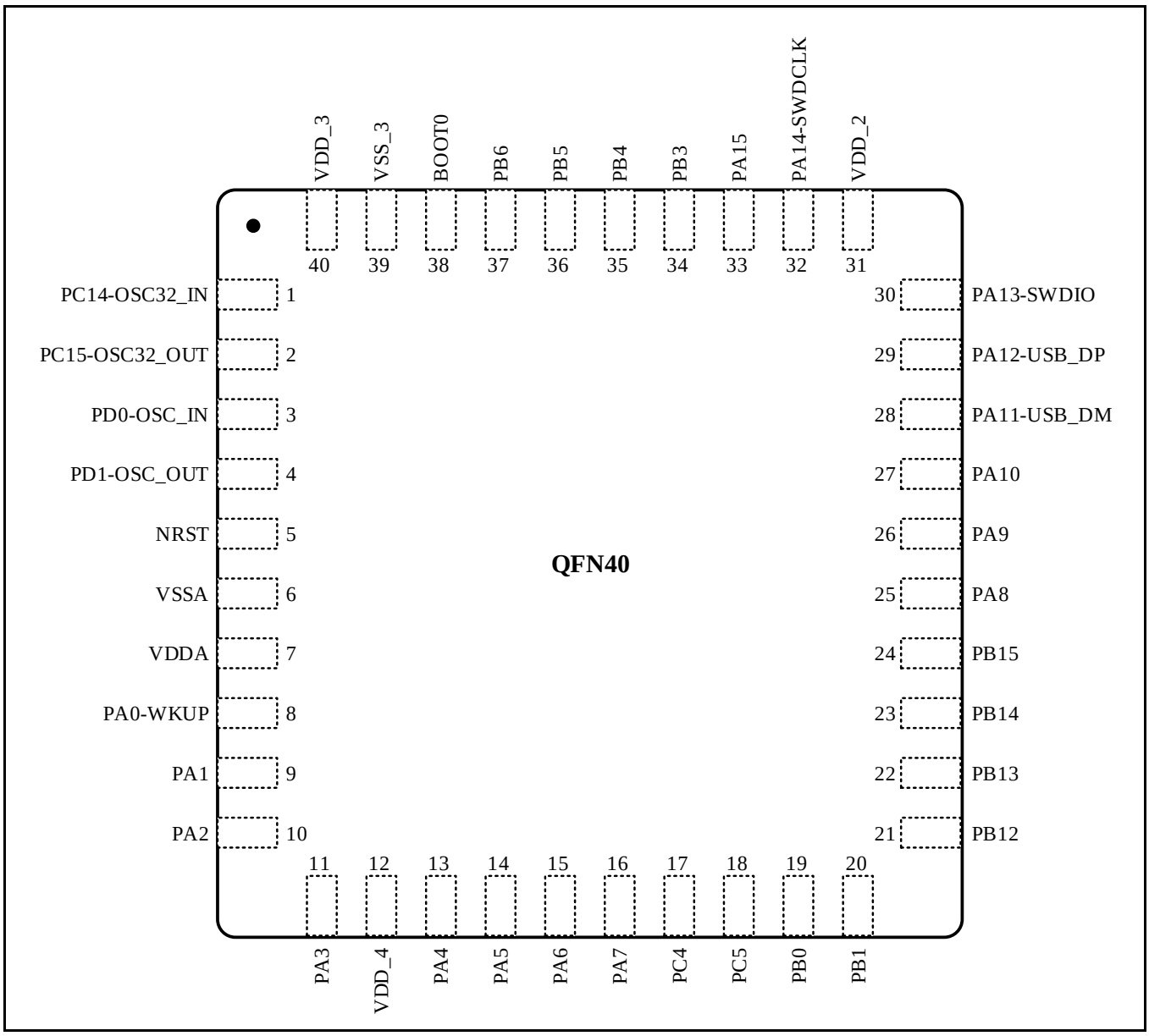
3.2 QFN40 package

3.2.1 QFN40 pin distribution



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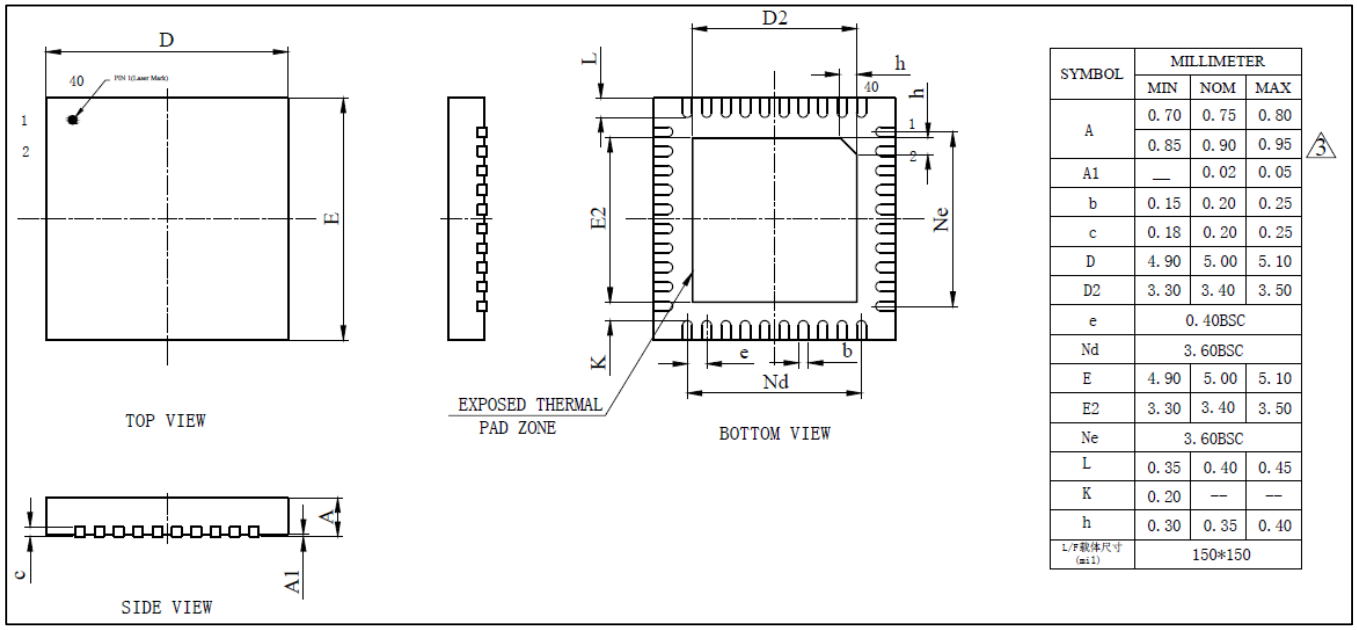
3.2.2 QFN40 package size



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.85	0.90	0.95
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.30	3.40	3.50
e	0.40BSC		
Nd	3.60BSC		
E	4.90	5.00	5.10
E2	3.30	3.40	3.50
Ne	3.60BSC		
L	0.35	0.40	0.45
K	0.20	—	—
h	0.30	0.35	0.40
L/F载体尺寸 (mil)	150*150		

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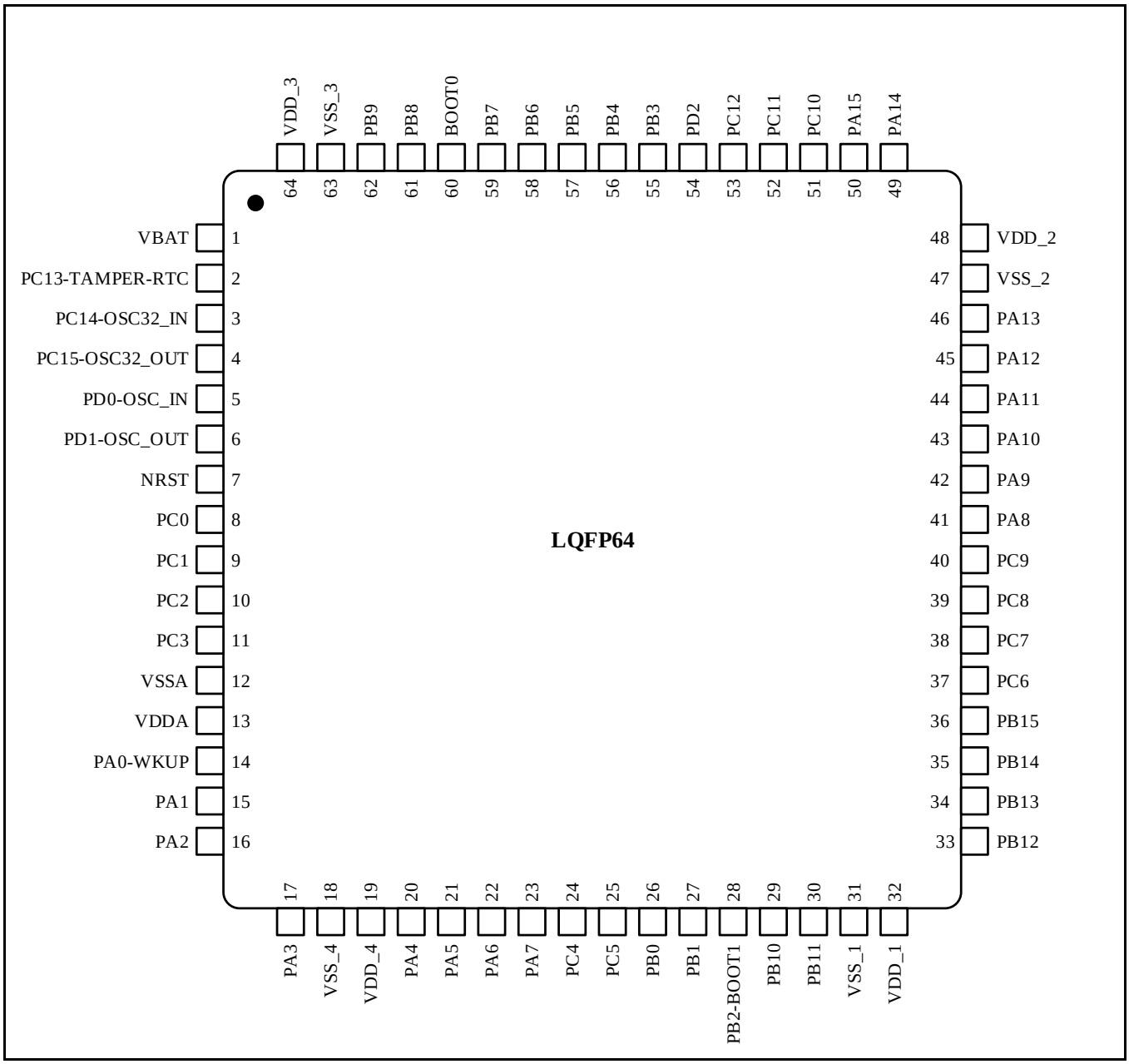
3.3 LQFP64 package

3.3.1 LQFP64 pin distribution



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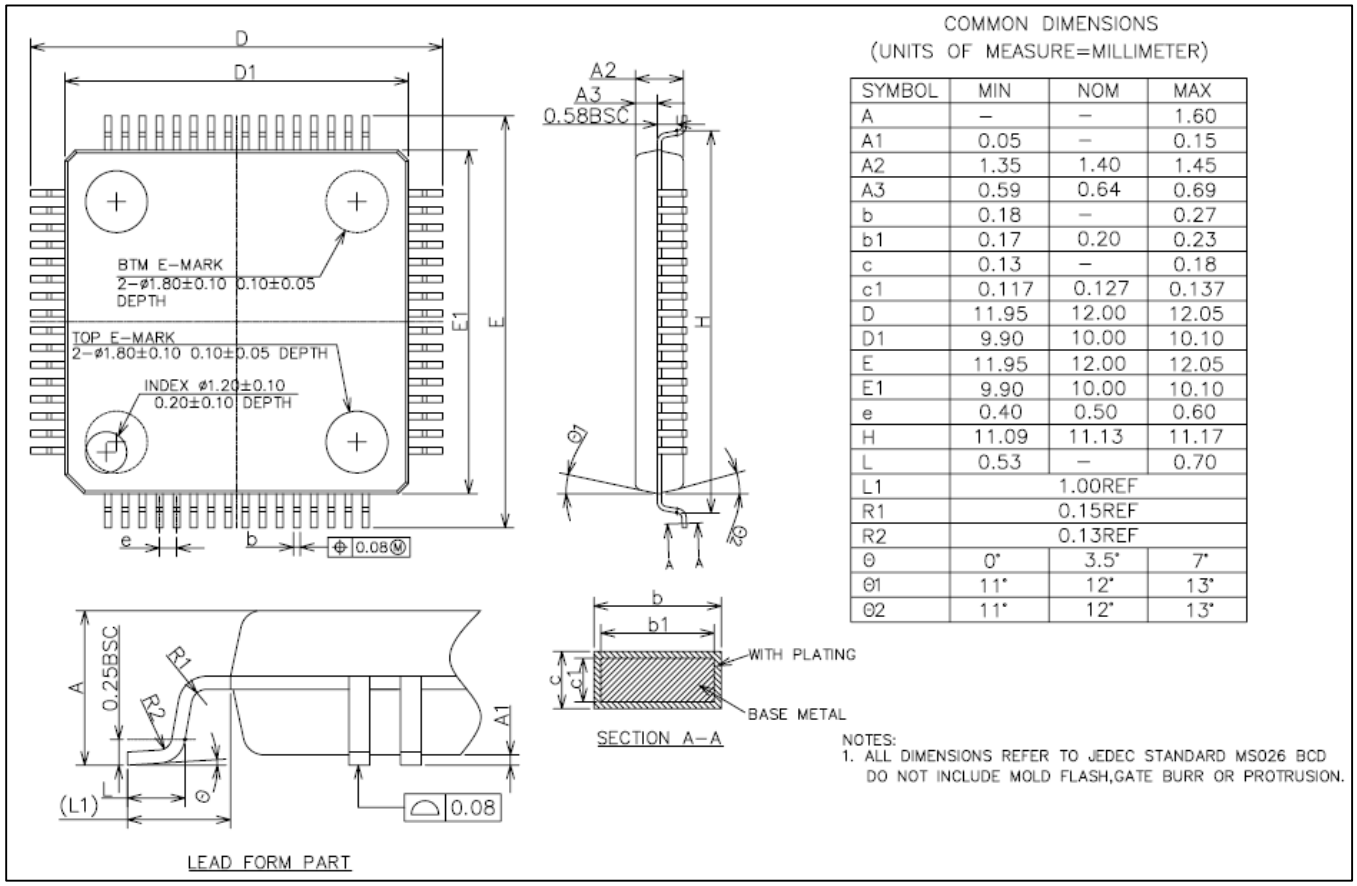
3.3.2 LQFP64 package size



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	–	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS026 BCD
DO NOT INCLUDE MOLD FLASH,GATE BURR OR PROTRUSION.

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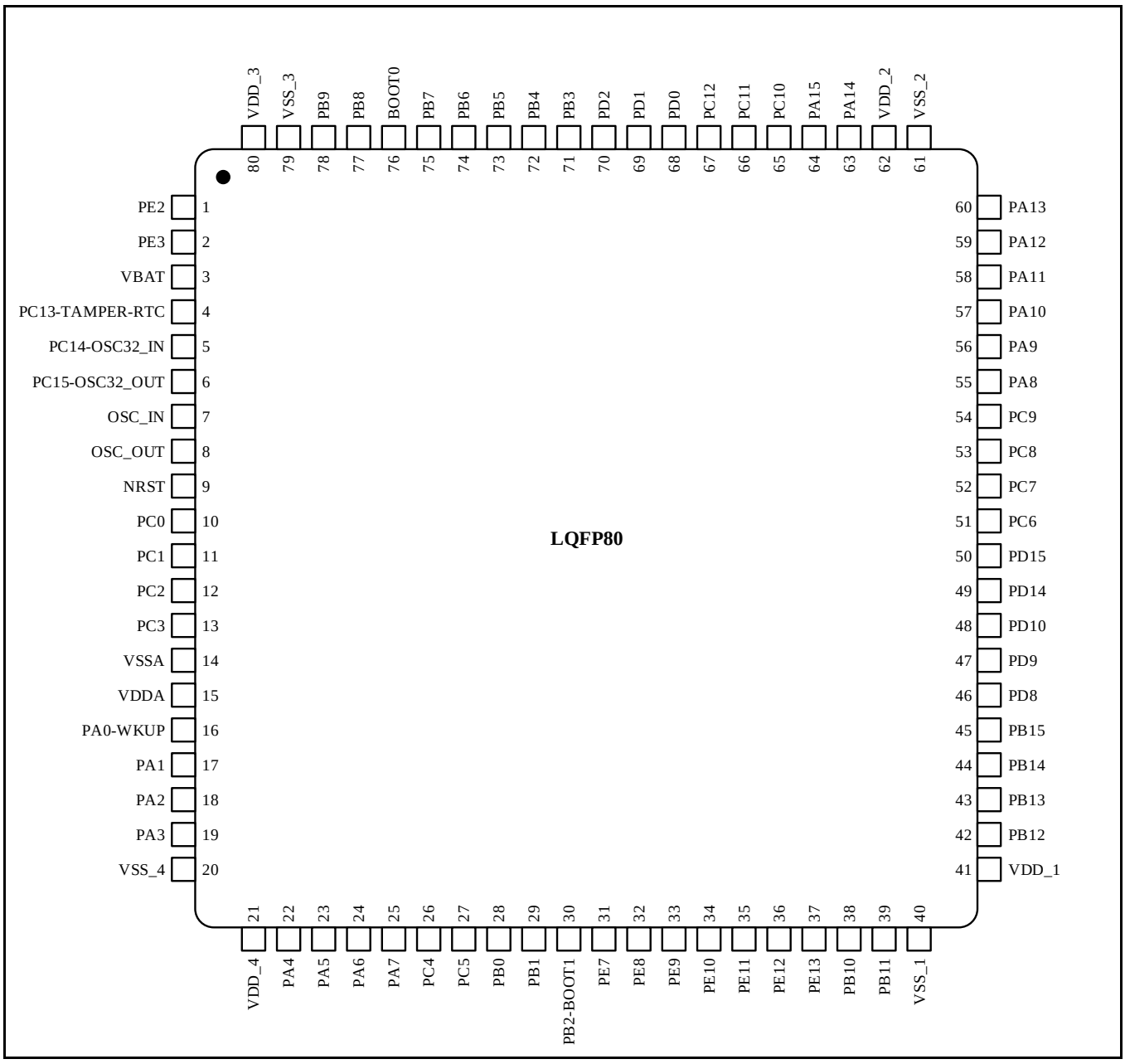
3.4 LQFP80 package

3.4.1 LQFP80 pin distribution



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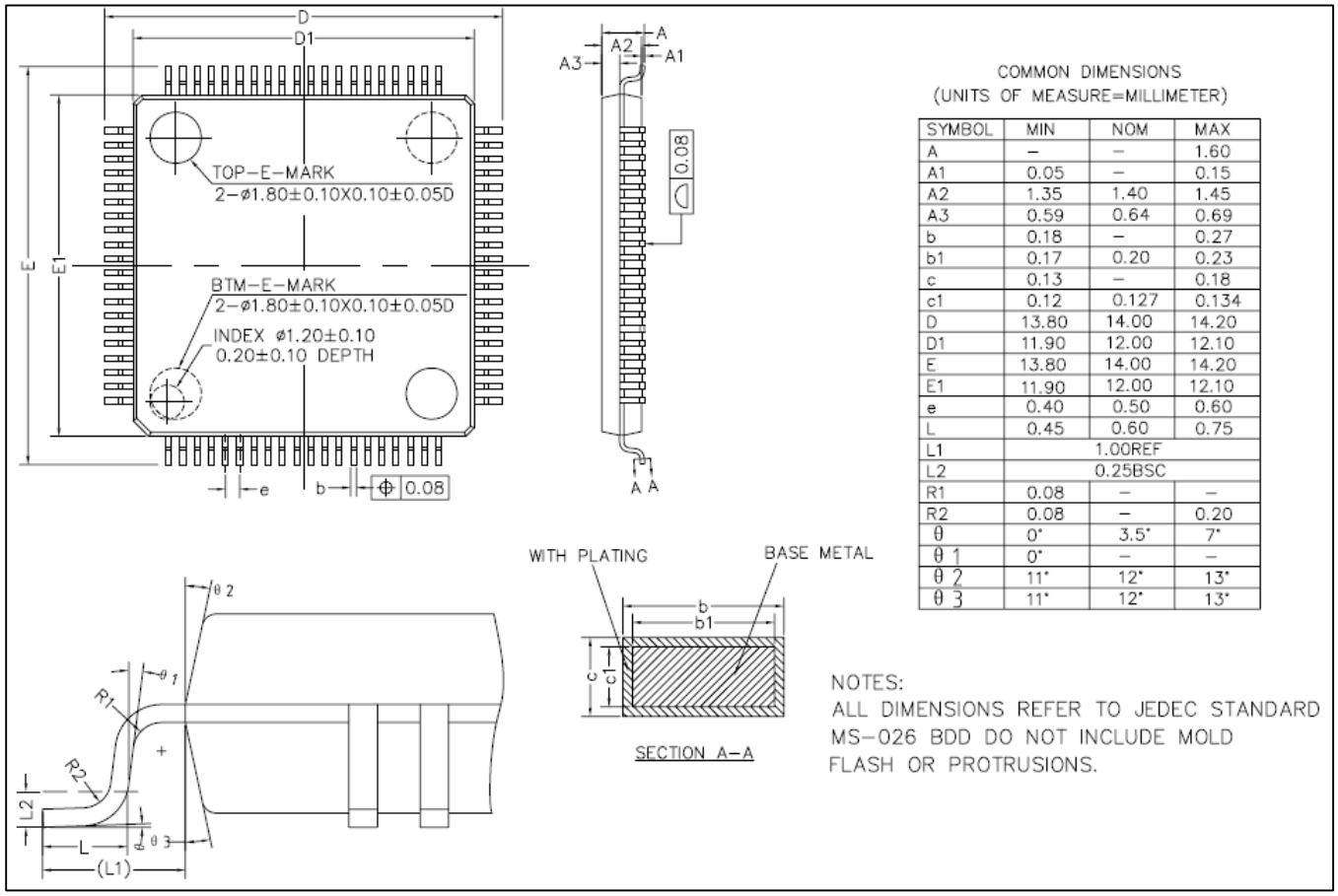
3.4.2 LQFP80 package size



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	–	–
R2	0.08	–	0.20
θ	0°	3.5°	7°
θ 1	0°	–	–
θ 2	11°	12°	13°
θ 3	11°	12°	13°

NOTES:
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4 Version history

Version	The date	Note
V1.0	2020.2.12	New document
V1.0.1	2020.12.15	1. Modify 3.1.1, 3.2.1, 3.3.1, 3.4.1 pin distribution diagram
V1.1	2022.7.6	1. Delete SDIO eMMC format
V1.2.0	2024.11.19	1. Modify Naming rules to Ordering information, modify ordering information table

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