

# N32A455xxL8 series

# Product Brief

**N32A455xxL8 series based on 32-bit ARM Cortex-M4F kernel, run up to 72MHz, support floating-point unit and DSP instructions, integrates up to 512KB embedded flash, 144KB SRAM, integrates rich high-performance analog devices, built-in 4x 12bit 4.2Msps ADCs, 4x independent rail-to-rail operational amplifiers, 7x high-speed comparators, 2x 1Msps 12bit DACs, integrates multi-channel U(S)ART, I2C, SPI, QSPI, CAN, SDIO communication interfaces, built-in cryptographic algorithm hardware acceleration engine**

## Key features

- **CPU core**
  - 32-bit ARM Cortex-M4 core + FPU, single-cycle hardware multiply and divide instructions, DSP instruction and MPU support
  - Built-in 8KB instruction Cache, support Flash acceleration unit execution program 0 wait
  - Maximum main frequency 72MHz, 90DMIPS
- **Memory**
  - Up to 512KByte on-chip Flash with encrypted storage, partition management and data protection, hardware ECC checksum, 100,000 erasures, 10-year data retention
  - Up to 144KByte on-chip SRAM (including 16KByte Retention RAM) with hardware parity support
- **High-performance analog interface**
  - 4x 12bit 4.2Msps high-speed ADCs, configurable in 12/10/8/6-bit mode, with sampling rates up to 9Msps in 6bit mode, up to 38 external single-ended input channels, supporting differential mode
  - 4x rail-to-rail operational amplifiers with built-in programmable gain amplification up to 32x
  - Up to 7 high-speed analog comparators with built-in 64-level adjustable comparison reference
  - 2x 12-bit DACs with 1Msps sampling rate
  - Support external input independent reference voltage source
  - All analog interfaces support 1.8~3.6V full voltage operation
- **Clock**
  - 4MHz~32MHz External High Speed Crystal
  - 32.768KHz External Low Speed Crystal
  - Internal High Speed RC 8MHz
  - Internal low-speed RC 40KHz
  - Internal high speed PLL
  - Support 1 channel clock output, configurable system clock, HSE, HSI or PLL post-division output
- **Reset**
  - Support power-up/power-down/external pin reset

- Support programmable low voltage detection and reset
- Support watchdog reset
- **Support up to 80 GPIOs with multiplexing function and a maximum flip speed of 50MHz**
- **Communication interface**
  - 7x U(S)ART interfaces, up to 4.5 Mbps, including 3 USART interfaces (1xISO7816, 1xIrDA, LIN supported) and 4 UART interfaces
  - 3x SPI interfaces with speeds up to 36 MHz, 2 of which support I2S
  - 1x QSPI interface with speeds up to 144 Mbps
  - 4x I2C interfaces at up to 1 MHz, master-slave mode configurable, dual address response support in slave mode
  - 2x CAN 2.0A/B bus interfaces
  - 1x SDIO interface, supporting SD/SDIO/MMC format
- **2x high-speed DMA controllers, each controller supports 8 channels, channel source and destination**
- **RTC real time clock, support leap year perpetual calendar, alarm events, periodic wake-up, support internal and external clock calibration**
- **Timer counter**
  - 2x 16-bit advanced timer counters, support input capture, complementary output, quadrature encoding input, etc., with maximum control accuracy of 13.9ns; each timer has 4 independent channels, 3 of which support 6 complementary PWM outputs
  - 4x 16bit general-purpose timers, each timer has 4 independent channels, support input capture/output comparison/PWM output
  - 2x 16bit base timer counters
  - 1x 24bit SysTick
  - 1x 7bit Window Watchdog (WWDG)
  - 1x 12bit Independent Watchdog (IWDG)
- **Programming mode**
  - Support SWD/JTAG online debugging interface
  - Support UART bootloader
- **Safety features**
  - Built-in hardware acceleration engine for cryptographic algorithms
  - Support DES/3DES、AES、SHA1/SHA224/SHA256、SM1、SM3、SM4、SM7、MD5 algorithms
  - Flash storage encryption, multi-user partition management (MMU)
  - TRNG true random number generator
  - CRC16/32 operation
  - Support write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)

- Support program encryption download
- Support clock failure detection, tamper-proof detection
- **96-bit UID and 128-bit UCID**
- **Working Conditions**
  - Working voltage range: 1.8V~3.6V
  - Working temperature range: -40°C~125°C
  - Certified by AEC-Q100-G2
  - ESD:  $\pm 4\text{KV}$  (HBM model),  $\pm 1\text{KV}$  (CDM model)
- **Package**
  - LQFP48(7mm x 7mm)
  - LQFP64(10mm x 10mm)
  - LQFP100(14mm x 14mm)

# 1 Ordering information

Figure 1-1 N32A455 Series Part Number Information

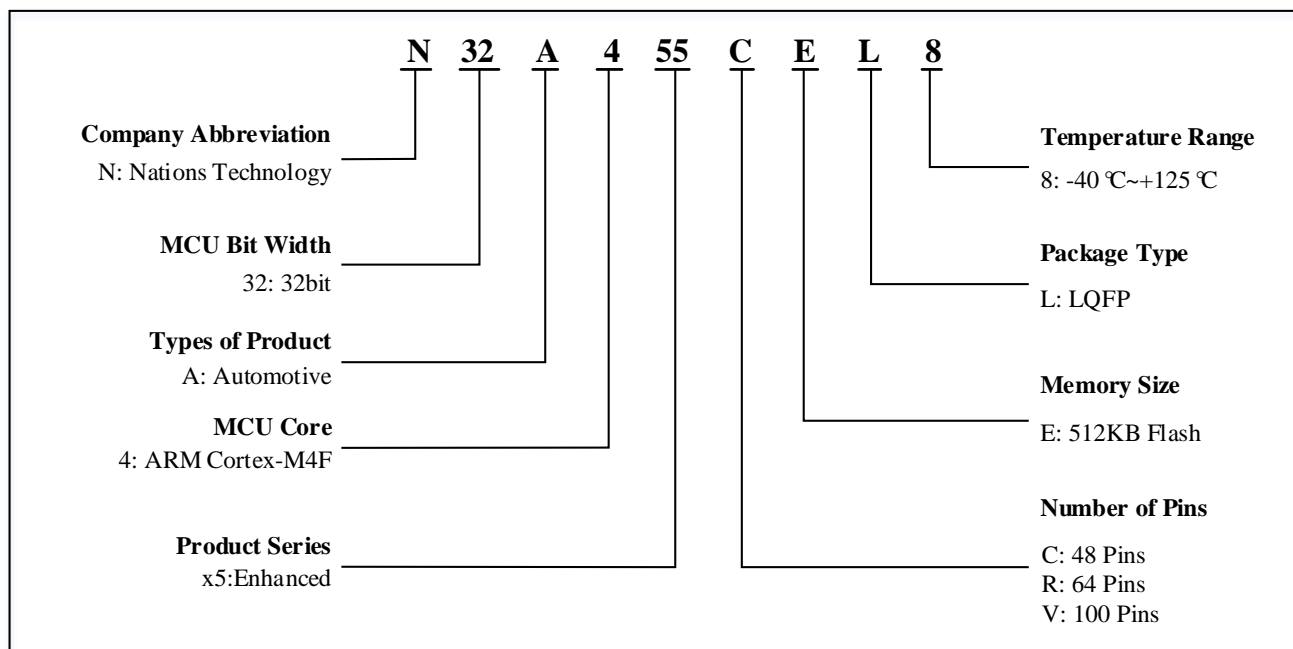


Table 1-1 N32A455 Series Ordering Code

Ordering code <sup>(1)</sup>	Package	Package size	Packaging <sup>(2)</sup>	SPQ <sup>(3)</sup>	Temperature range
N32A455CEL8	LQFP48	7mm*7mm	Tray	250	-40°C ~ 125°C
N32A455REL8	LQFP64	10mm*10mm	Tray	160	-40°C ~ 125°C
N32A455VEL8	LQFP100	14mm*14mm	Tray	90	-40°C ~ 125°C

- For the latest detailed ordering information, please refer to the Selection Guide.
- The packaging provided is the basic packaging. If user has any other requirements, please contact Nations.
- Minimum packaging quantity.

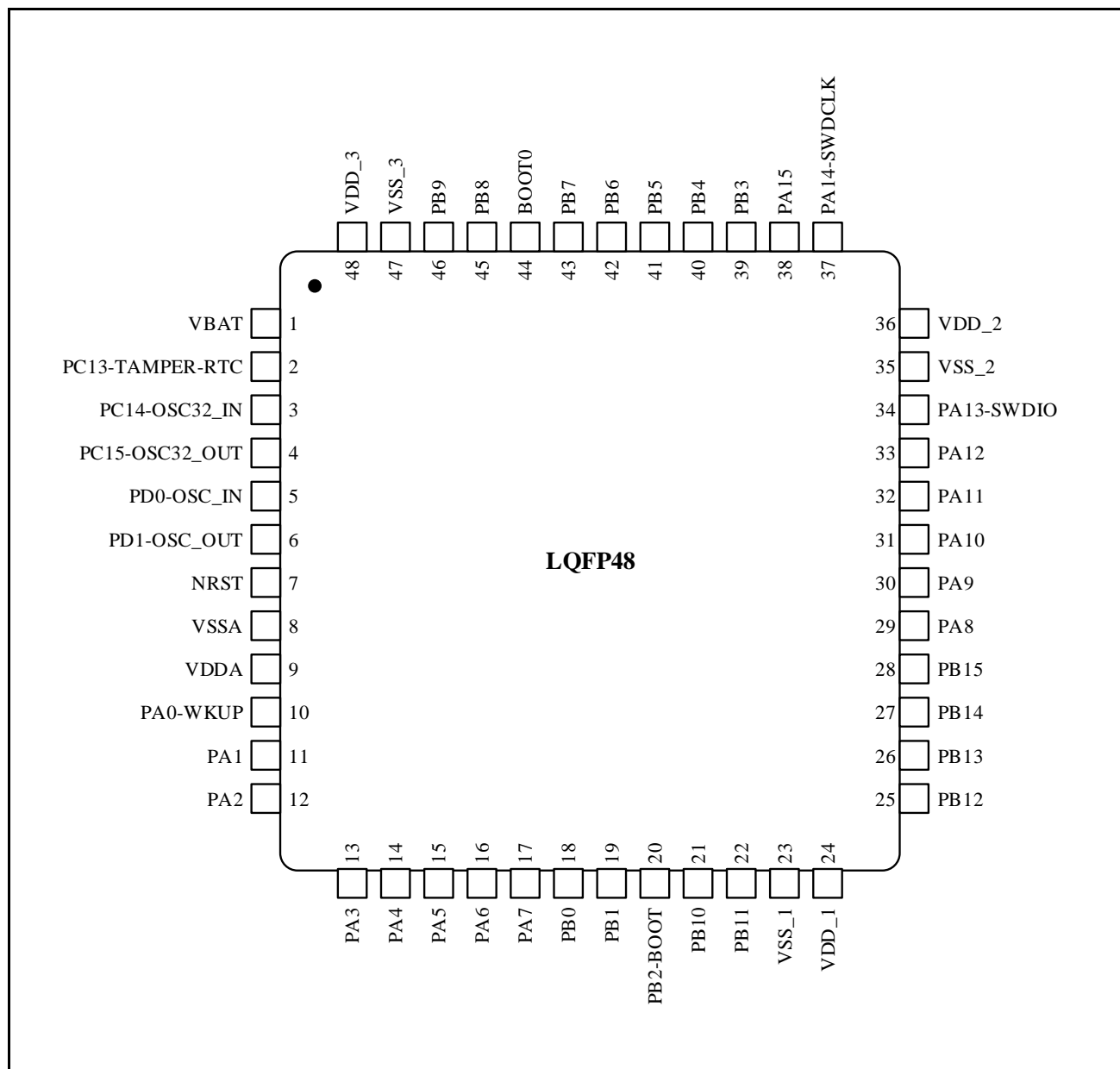
## 2 List of devices

Part number		N32A455CEL8	N32A455REL8	N32A455VEL8
Flash capacity (KB)		512		
SRAM capacity (KB)		144		
CPU frequency		ARM Cortex-M4 @72MHz,90 DMIPS		
Working environment		1.8~3.6V/-40~125℃		
Timer	General	4		
	Advanced	2		
	Basic	2		
Communication interface	SPI	3		
	I2S	2		
	QSPI	Only Single Wire	1	
	I2C	3	4	
	USART	3		
	UART	3	4	
	CAN	2		
	SDIO	No	1	
GPIO		37	51	80
DMA		2		
Number of Channels		16Channel		
12bit ADC		4	4	4
Number of channels		16Channel	22Channel	38Channel
12bit DAC		2		
Number of channels		2Channel		
OPA/COMP		4/5	4/7	4/7
Algorithm support		DES/3DES、AES、SHA1/SHA224/SHA256、SM1、SM3、SM4、SM7、MD5、CRC16/CRC32、TRNG		
Security protection		Read-write protection (RDP/WRP), Storage encryption, Partition protection, Secure startup		
Package		LQFP48	LQFP64	LQFP100

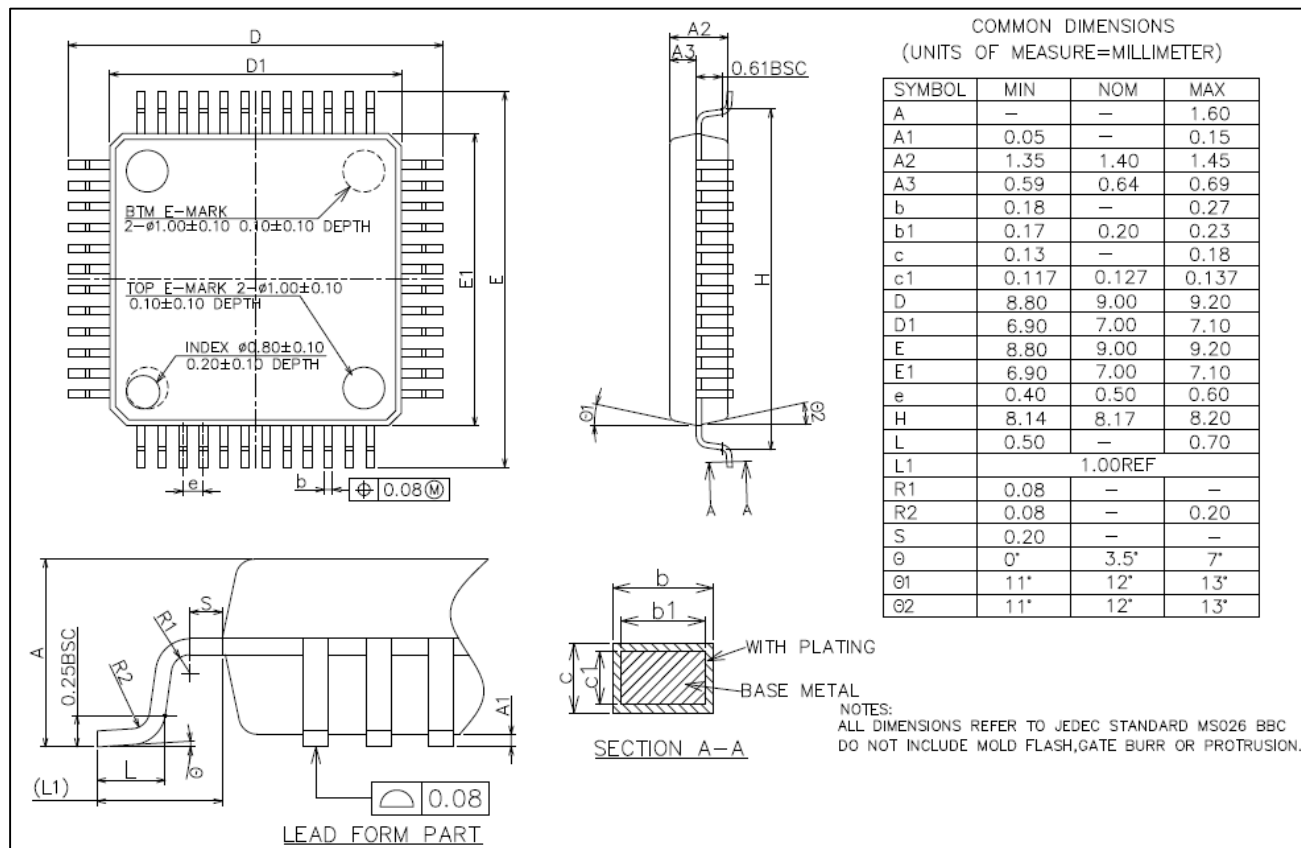
### 3 Package Information

#### 3.1 LQFP48 package

##### 3.1.1 LQFP48 pinouts

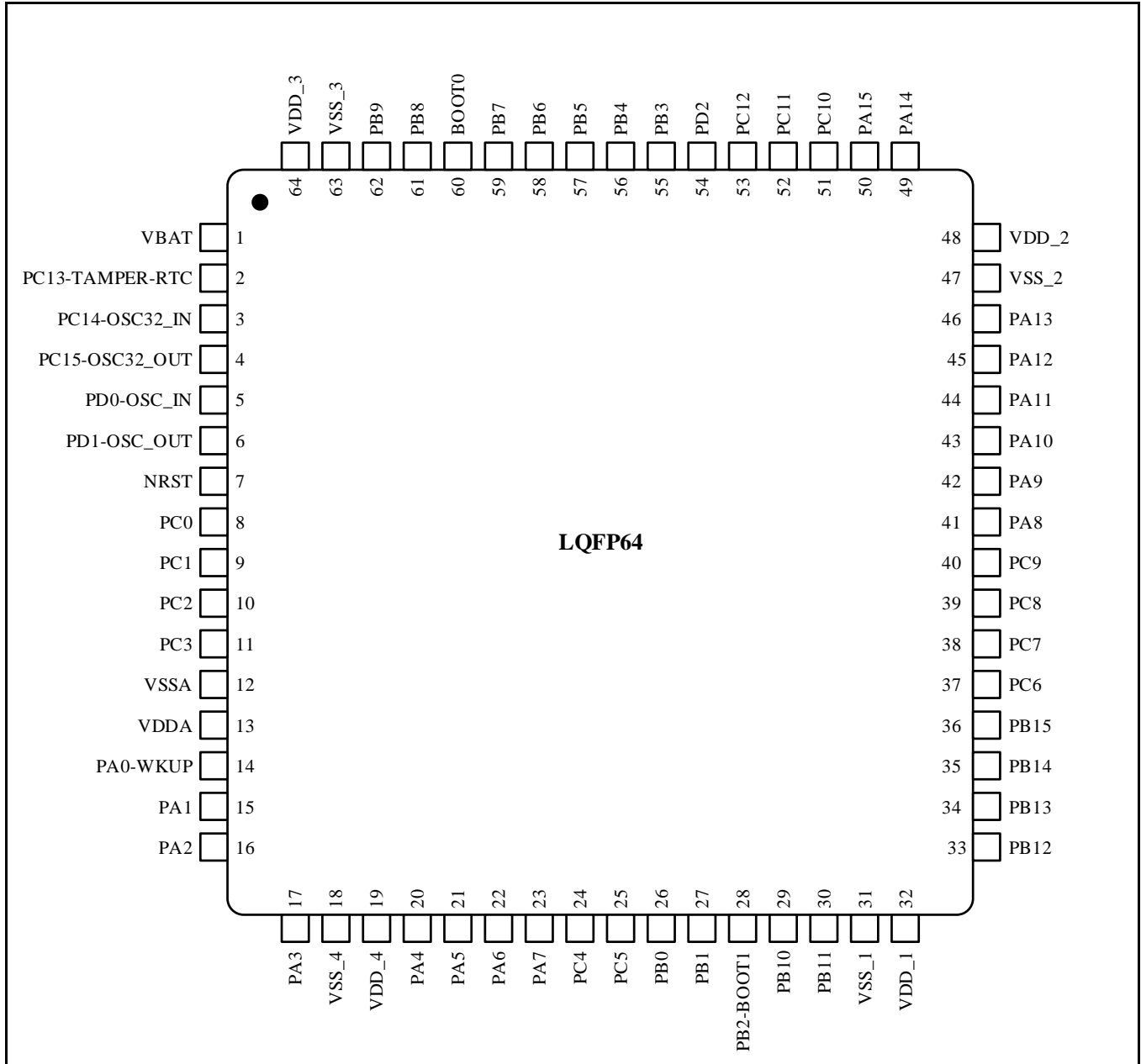


### 3.1.2 LQFP48 package outline



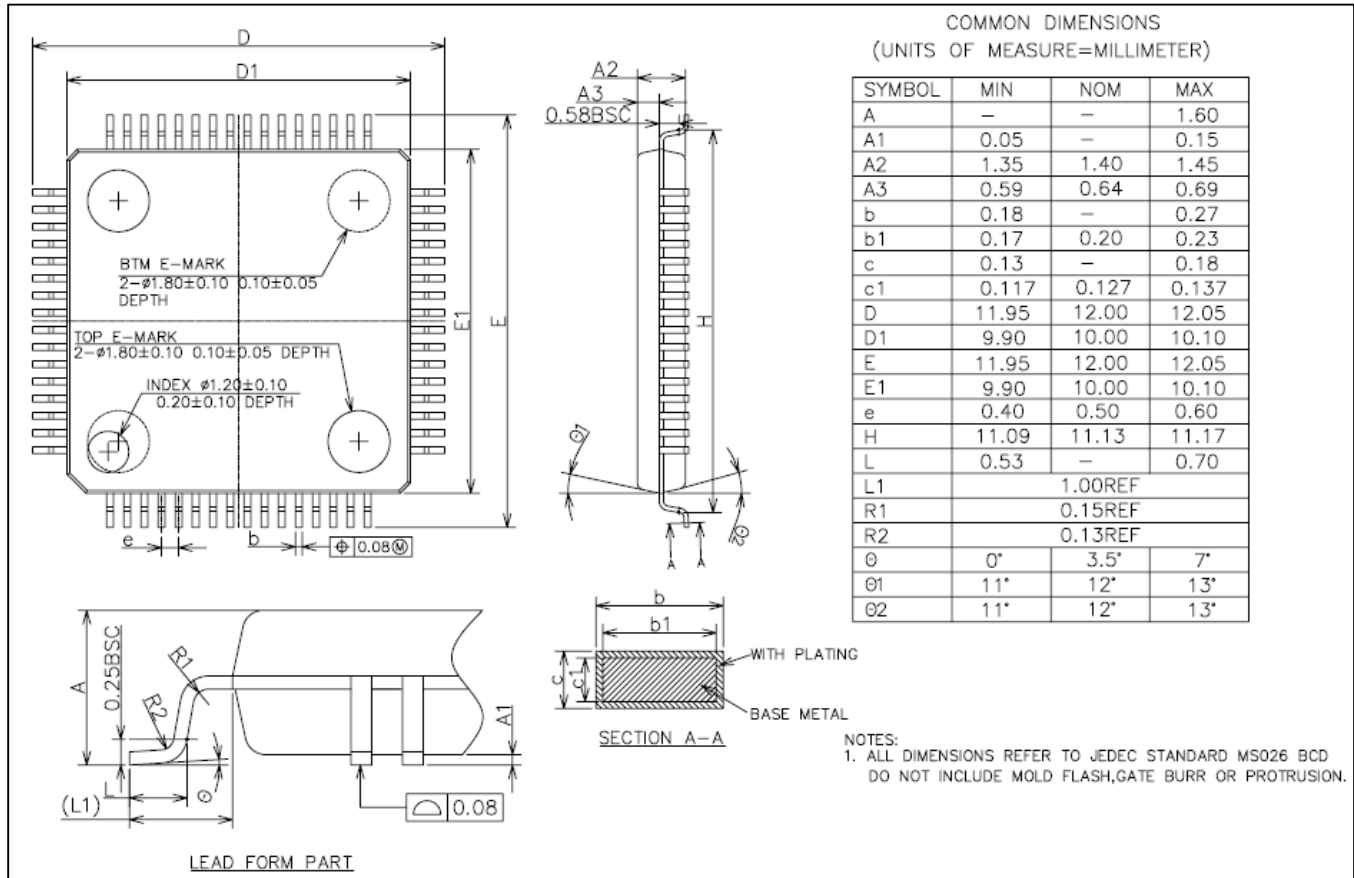
## 3.2 LQFP64 package

### 3.2.1 LQFP64 pinouts



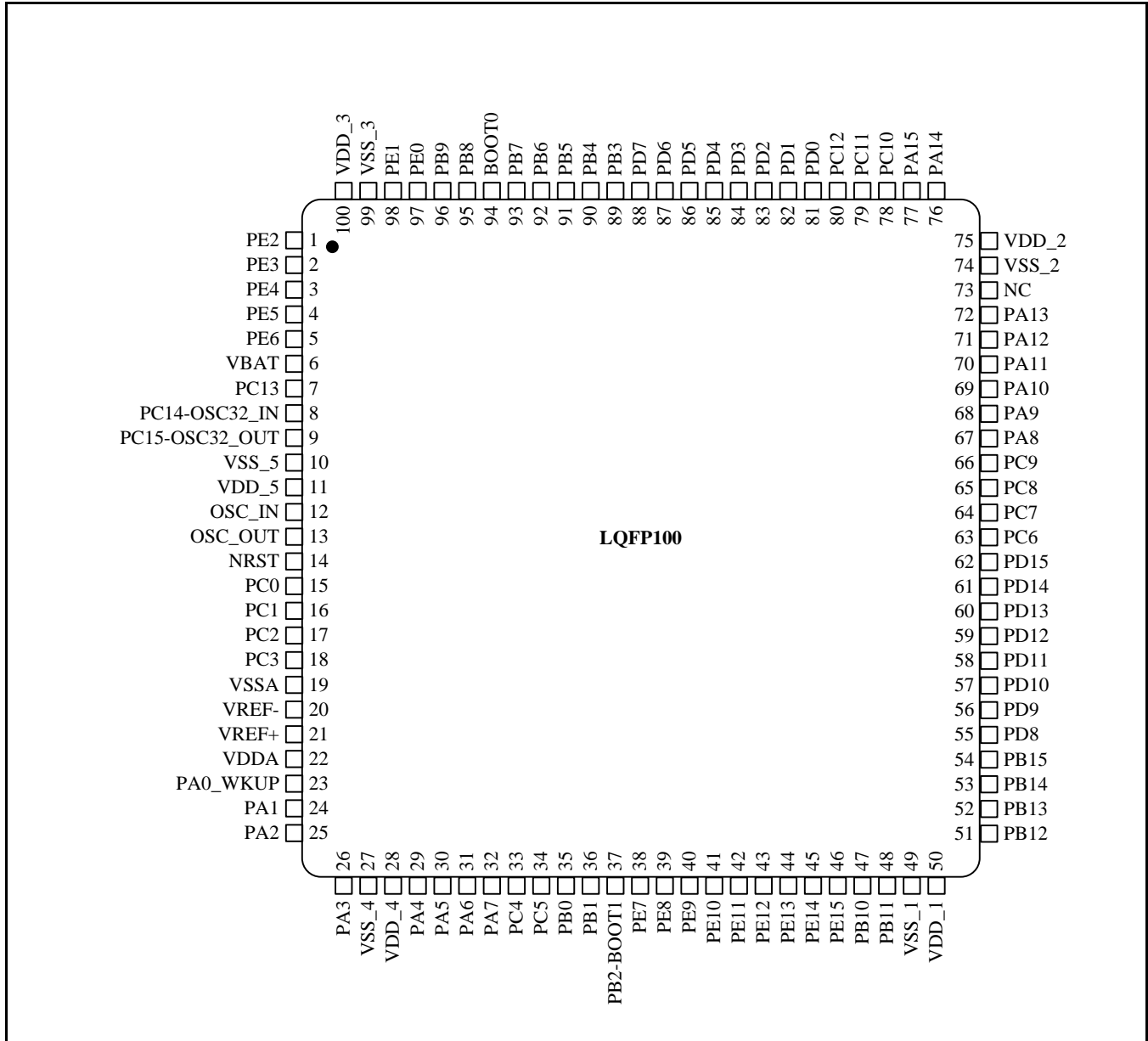


### 3.2.2 LQFP64 package outline

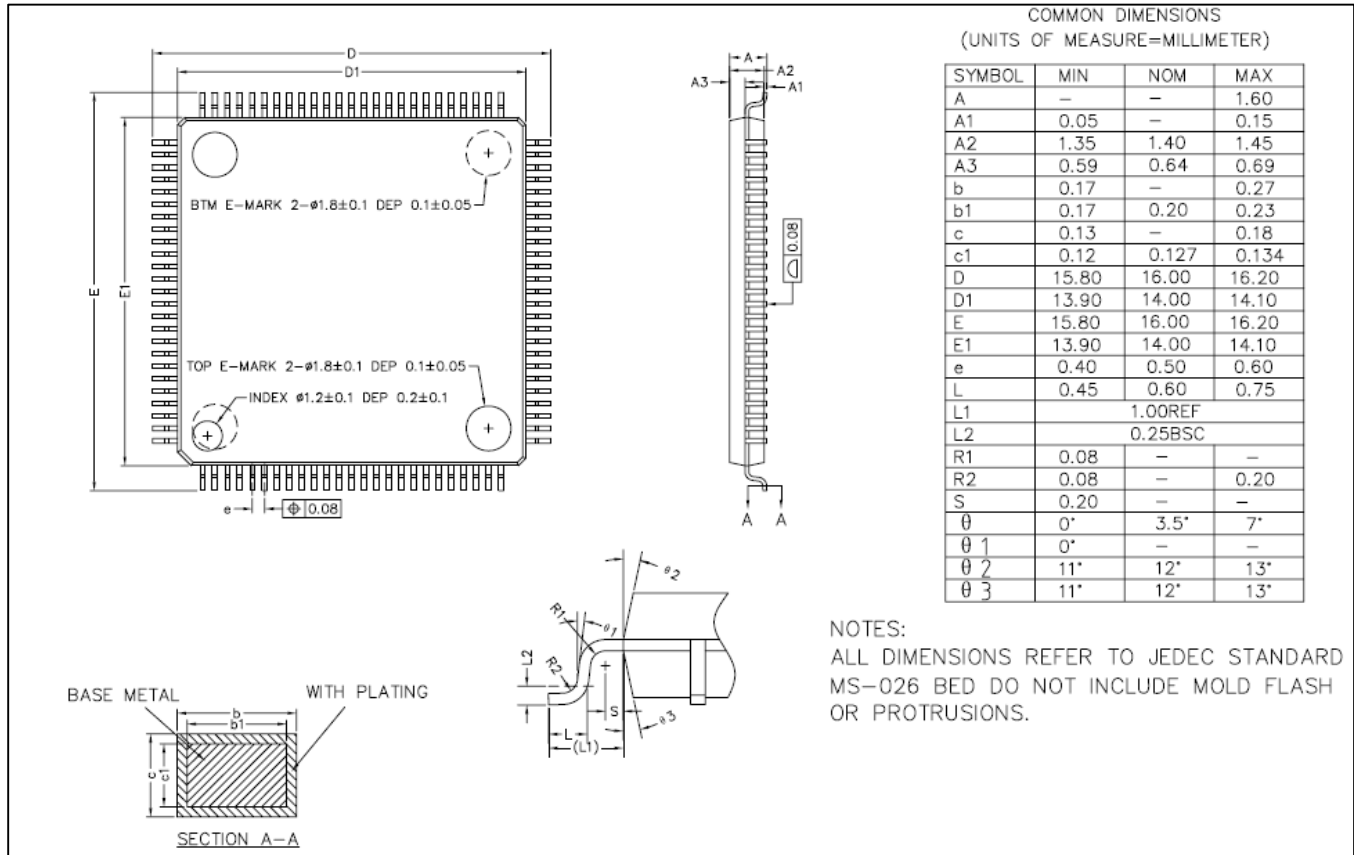


### 3.3 LQFP100 package

#### 3.3.1 LQFP100 pinouts



### 3.3.2 LQFP100 package outline



## 4 Version History

Date	Version	Remarks
2023.09.18	V1.0.0	Initial version
2024.11.20	V1.1.0	1. Modify Naming rules to Ordering information, modify ordering information table

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