Design guide

N32H47X/N32H48X series hardware design guide

Introduction

This document details the N32H47X/N32H48X series MCU hardware design checklist to provide users with hardware design guidance.

Table of contents

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1. N32H47X/N32H48X Series MCU Hardware Design Checklist

1.1 Introduction to Power Supply

The operating voltage (VDD) of the N32H47X/N32H48X series chips is 1.8V~3.6V. Mainly include: VDD, VDDA, VBAT pins. Please refer to the relevant data sheet for details.

1.2 VDD Power supply solution

VDD is the main power supply of the MCU and must be powered by a stable external power supply. The voltage range is 1.8V~3.6V. All VDD pins need to be placed with a 0.1uF decoupling capacitor nearby, and one of the VDD pins needs to be added with a 4.7uF decoupling capacitor. For the specific design of decoupling capacitors, please refer to the minimum system reference design schematic diagram of each package in Chapter 3.

VDDA is an analog power supply that provides power for ADC, DAC, COMP, and PGA. It is recommended to place a 0.1uF and a 2.2uF capacitor on the VDDA input pin.

VREF+ is the reference voltage, which provides the reference level for ADC and DAC. When VERF+ uses the built-in reference source VREFBUF, it is recommended to place a 0.1uF and a 1uF capacitor nearby the VREF+ pin. When VERF+ is powered externally, it is recommended to place a 0.1uF and a 2.2uF capacitor nearby the VREF+ pin.

1.3 Backup battery

The VBAT pin mainly supplies power to the backup power domain (RTC, LPTIM, Backup SRAM), so that the backup power domain module can still operate normally when the main power supply (VDD) is turned off.

1.4 External pin reset circuit

A system reset occurs when a low level (external reset) occurs on the NRST pin. The external NRST pin reset reference circuit is as follows.

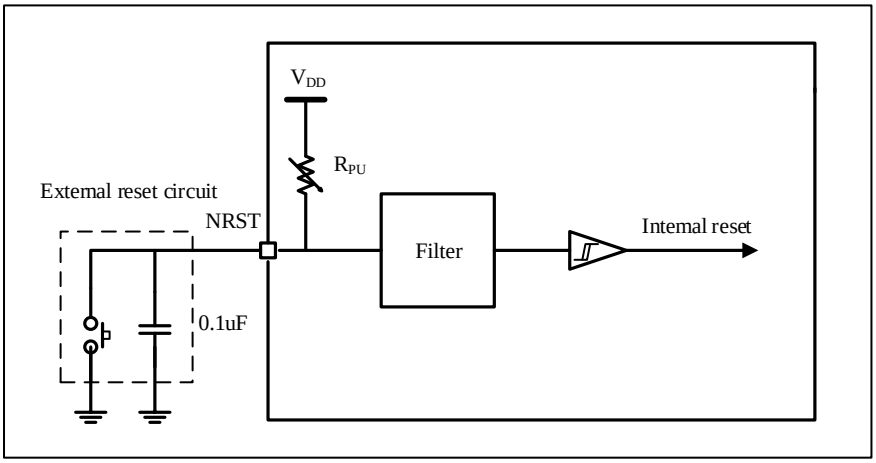

Figure 1-1 System reset diagram

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Note: It is recommended that the reset pin NRST is not left floating during design. The external capacitor 0.1uF is given as a typical reference value. If the reset time needs to be accelerated, the NRST pin can be externally pulled up. In addition, the user can decide whether to add a reset button according to the actual needs of the product.

1.5 External clock circuit

The N32H47X/N32H48X series MCUs contain 2 external clocks: external high-speed clock HSE (4MHz~32MHz) and external low-speed clock LSE (usually 32.768KHz).

HSE and LSE configure corresponding load capacitance according to the characteristics of the crystal oscillator. For details, please refer to the description of external clock characteristics in the relevant data sheet.

1.6 Boot Pin Connection

The figure below shows the external connections required when the N32H47X/N32H48X series chips select boot memory. For information on startup mode, please refer to the relevant chapters of the user manual.

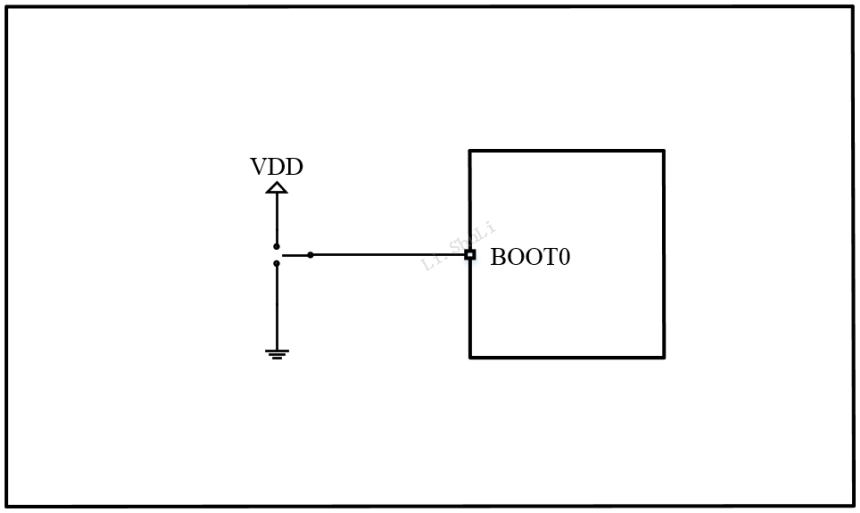

Figure 1-2 Implementation example of startup mode

When the BOOT pin is pulled high, the chip starts from the BOOT area after reset; when the BOOT pin is pulled low, the chip starts from the user area after reset.

1.7 ADC Converter.

Regarding DC circuit design, please pay attention to the following points:

1） When using ADC sampling, it is recommended to shorten the external wiring distance of the ADC sampling channel;

2） It is recommended that the input signal of the ADC be kept away from some high-frequency flip signals;

3） Note the maximum supported rates for slow channel and fast channel:

When the ADC input clock of the N32H47X/N32H48X series is 80MHZ, the ADC fast channel sampling

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rate does not exceed 4.7Msps, and the ADC slow channel sampling rate is recommended to not exceed 2.5Msps;

4） During ADC conversion, the chip does not support modifying the ADC configuration. If you need to modify the configuration, you need to wait for the current conversion to end or turn off the ADC before configuring;

5） When using a certain ADC channel, you cannot apply negative voltage (such as -0.2V) to other unused ADC sampling channels. If this negative voltage is applied, the voltage of the ADC channel for normal sampling will be pulled down, resulting in the reading of Data is inaccurate;

6） When using a certain ADC channel, do not apply high voltage (greater than the VDD voltage) to other unused ADC sampling channels. If this high voltage is applied, the voltage of the ADC channel for normal sampling will be pulled up, causing the read data to be incorrect. allow;

7） When using ADC, the sampling rate of ADC is related to RAIN. The smaller the RAIN, the faster the sampling rate. See the table below for details:

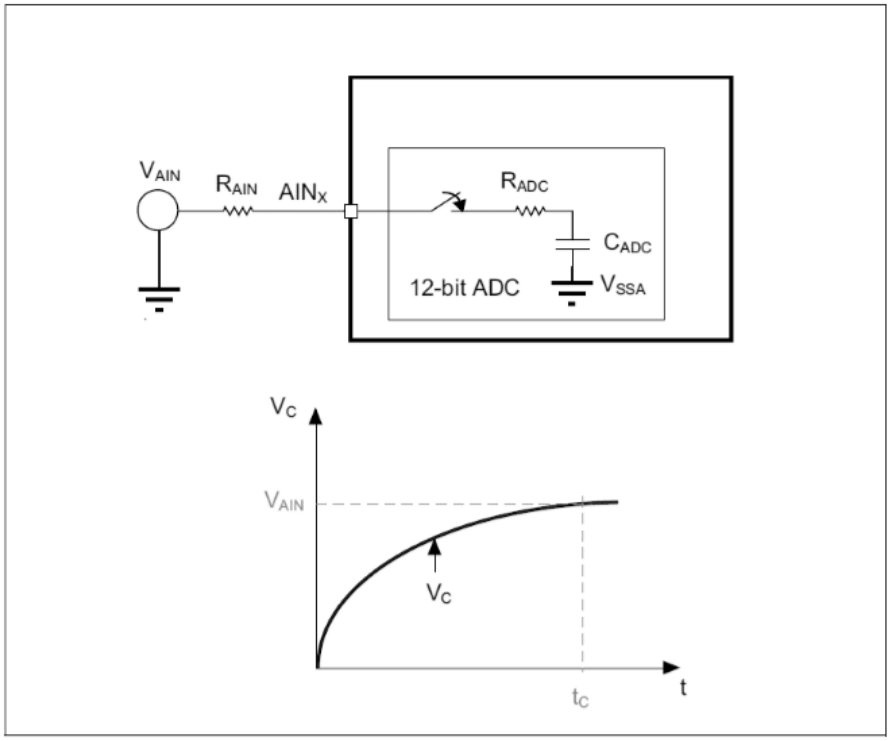

Figure 1-3 Influence of series resistance of ADC input port

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ADC sampling schedule:

Resolution	R_{AIN}（kΩ）	Minimum sampling time（ns）	
		Fast track	Slow channel
12-bit	0.14	45.0	73.0
	0.6	79.0	103.0
	4.6	300.0	345.0
	9.5	576.0	651.0
	19	1131.0	1257.0
	48	2776.0	3051.0
10-bit	0.14	39.0	61.0
	0.6	64.0	88.0
	4.6	250.0	357.0
	9.5	478.0	540.0
	19	935.0	1040.0
	48	2294.0	2526.0
8-bit	0.14	33.0	50.0
	0.6	52.0	71.0
	4.6	202.0	234.0
	9.5	391.0	457.0
	19	800.0	1012.0
	48	1838.0	2027.0
6-bit	0.14	27.0	40.0
	0.6	41.0	56.0
	4.6	153.0	177.0

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	9.5	292.0	330.0
	19	569.0	642.0
	48	1435.0	1666.0

Figure 1-4 ADC sampling schedule

1.8 PGA application reference

The N32H47X series chips contain 4 flexible programmable gain amplifiers (PGA). For details, please refer to the pin multiplexing definition in the corresponding data sheet. Any differential PGA can be split into two single-ended PGAs for independent use.

Note: N32H48X series chips do not support PGA.

1.8.1 Single-ended mode application

The single-ended mode application of PGA is shown in the figure below:

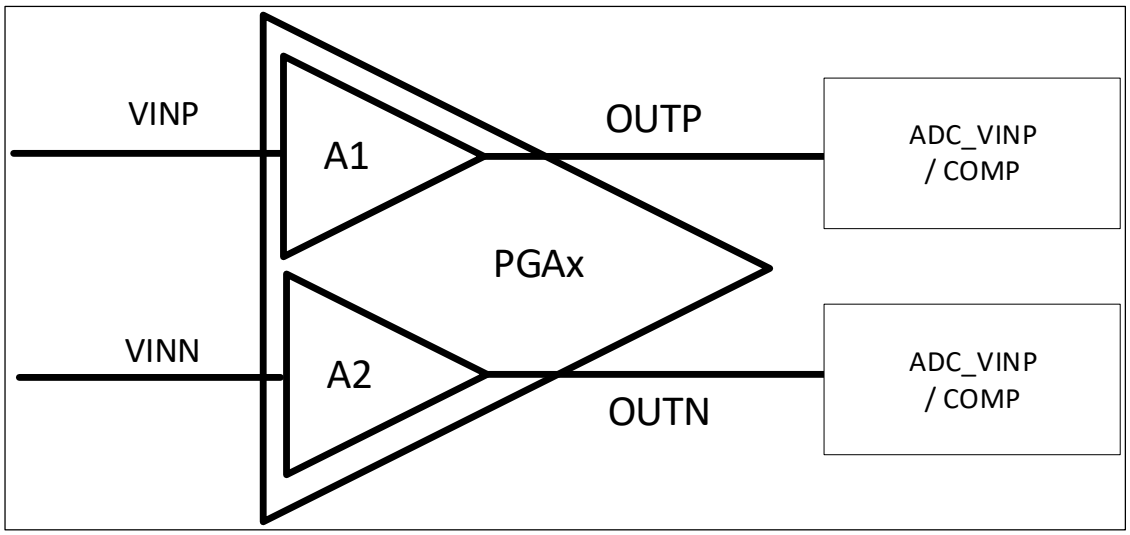

Figure 1-5 PGA single-ended working structure

At this time, a PGA will be split into two independent amplifiers, with each input corresponding to a separate output:

$$OUTP = A1 \times VINP$$

$$OUTN = A2 \times VINN$$

The amplification gains A1/A2 of the two amplifiers are configured individually through different registers. At this time, the output of the PGA can be connected to the comparator for work or to the positive input of the ADC for measurement.

The input to the PGA can come from external hardware configuration or the internal DAC output, with specific input channels selected through registers. The dotted box in the left half of Figure 1-4 is an example of hardware configuration.

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The small signal voltage that needs to be amplified is collected through current source C1/C2 and Rsense. It is pulled up to a suitable voltage suitable for amplification through the common mode Rcm, and then enters the PGA for amplification.

Note that the required resistance value Rcm >> Rsense.

1.8.2 Differential mode applications

In most cases, due to input noise and circuit parasitic parameters, using single-ended mode will produce larger errors. In this case, using differential mode can effectively improve the output accuracy. Its working mode is as follows:

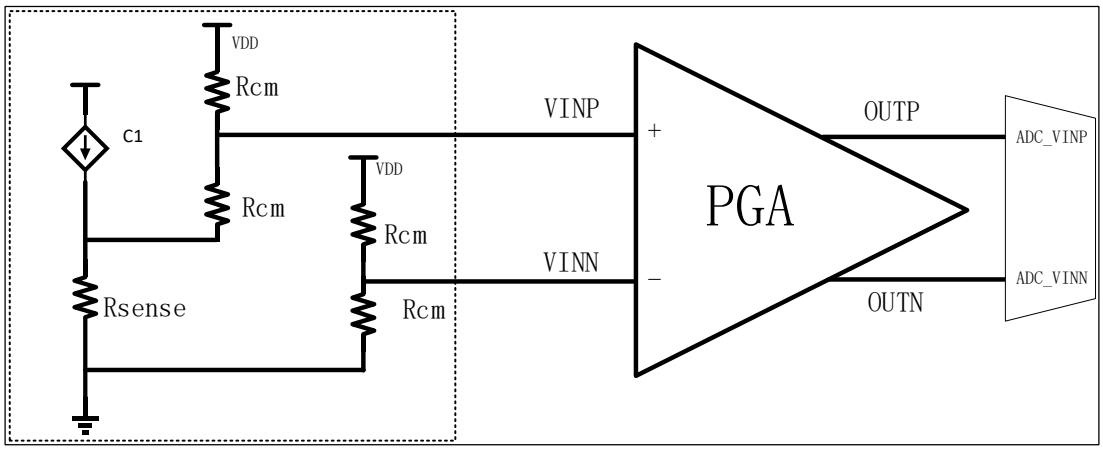

Figure 1-6 PGA differential working structure

In differential mode, the inputs at both ends will be differentially amplified through the PGA:

$$Voutp = Vinn + 1/2 \times A \times (Vinp - Vinn)$$

$$Voutn = Vinn - 1/2 \times A \times (Vinp - Vinn)$$

The gain A of the differential output is configured by a separate register, and the amplified differential signal enters the positive and negative terminals of the ADC for measurement at the same time.

The input to the PGA can come from external hardware configuration or the internal DAC output, with specific input channels selected through registers. The dotted box in Figure 1-5 shows an example of hardware configuration.

The small signal voltage that needs to be amplified is collected through the current source C1 and Rsense. The common mode voltage is provided through the common mode Rcm resistor division, and enters the PGA for differential amplification:

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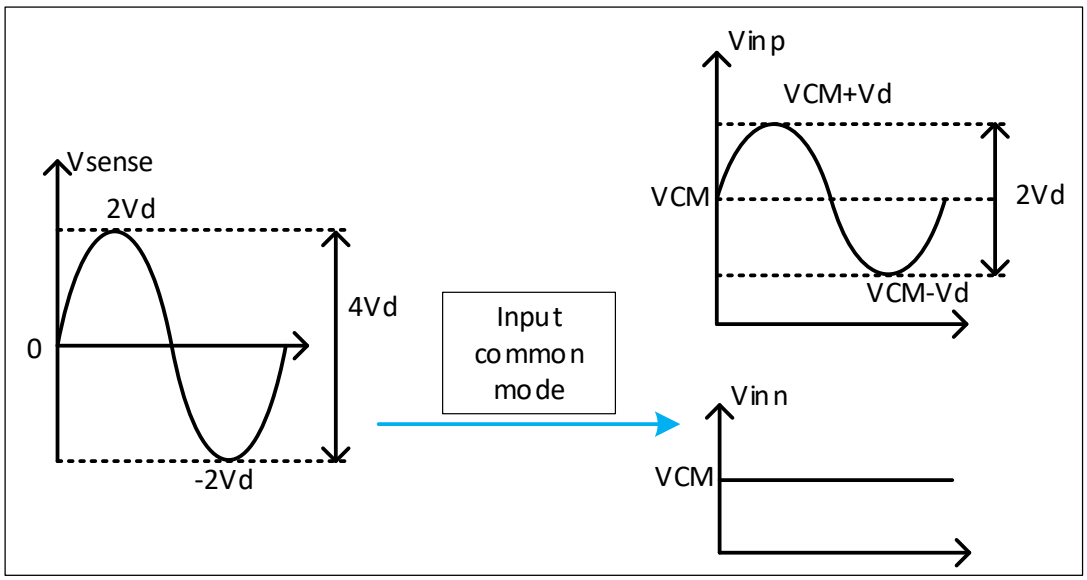

Figure 1-7 PGA differential input waveform

The design requires the resistance value Rcm >> Rsense, assuming Vsense generates a sine wave voltage with a swing amplitude of 4Vd. Both ends raise VCM respectively through the VDD voltage dividing circuit. Generally, VCM=VDD/2. At this time, VINN is a fixed voltage value of VCM, and VINN becomes a common-mode voltage VCM with a sine wave voltage with a swing of Vd. The raised voltage becomes the positive and negative inputs of the PGA.

The common-mode voltage VCM provided is necessary because the amplified output at both ends of the PGA must ensure that it is far away from the maximum swing or the minimum swing, otherwise it will cause a greater loss of accuracy.

After the signal enters the PGA and is amplified, it is output from both ends of OUTP/OUTN. Configure the PGA differential gain to be A. The input signal at both ends is amplified as shown in the figure:

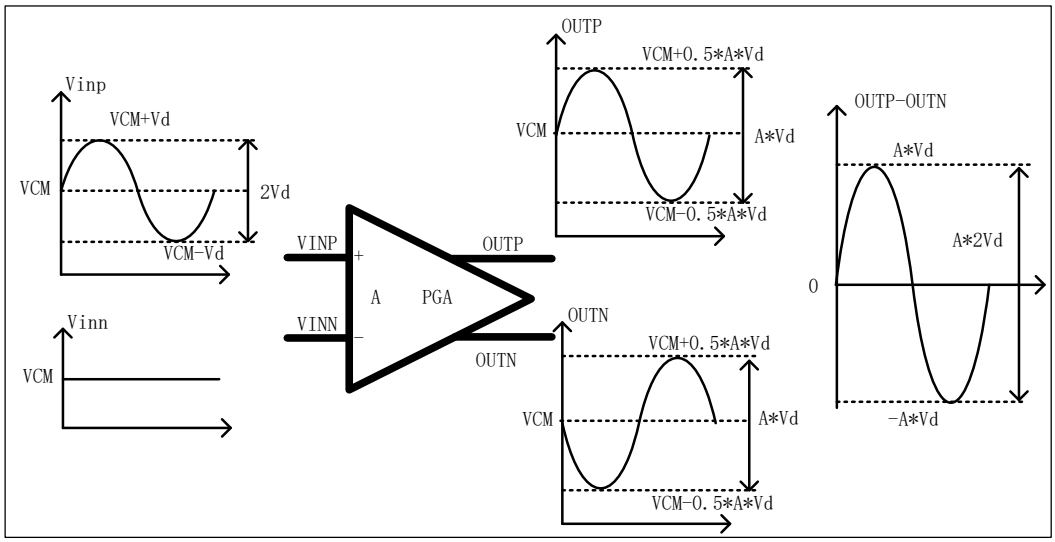

Figure 1-8 PGA differential amplification output waveform

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The differential output and input are given by the formula:

$$Voutp = Vinn + 1/2 \times A \times (Vinp - Vinn)$$

$$Voutn = Vinn - 1/2 \times A \times (Vinp - Vinn)$$

calculate. You can see:

The OUTP output is a constant common mode voltage, and the PN differential input is forward amplified by 0.5×A times.

The OUTN output is a constant common mode voltage, and the PN differential input is amplified by 0.5×A times in the negative direction.

The final signal entering the ADC is a signal with a common mode cancellation swing of A×2Vd, and the swing is A times larger than the input 2Vd.

At the same time, VCM ensures that the outputs at both ends are not close to the power supply and ground, and will not cause signal distortion.

1.8.3 Precautions for using PGA

To ensure the normal operation and accuracy of the PGA, please pay attention to the following points when using it:

1.To prevent output distortion, the input range in single-ended/differential mode should be considered based on gain and theoretical output voltage:

In single-ended mode, ensure: 0.3V <A×Vin < VDDA-0.3V

In differential mode, the output voltage Vout at each end must ensure 0.3V < OUTP/N < VDDA-0.3V,

2. The differential mode must provide a suitable common mode voltage VCM to the N terminal, usually VCM=VDDA/2.

1.9 IO power-on pulse processing

During the power-on process, due to the high-impedance state of the IO and the coupling characteristics of the internal circuit, a high-level pulse will appear on the IO at the moment of power-on (please measure the actual high pulse voltage value by the user). If this pulse will affect its application, it is recommended to hang an appropriate capacitor (1nF~100nF) or add an appropriate pull-down resistor (10K~100K) on the corresponding IO.

The following picture shows the IO (PB12) waveform diagram during the power-on process of the development board N32H473CEU7_STB_V1.0:

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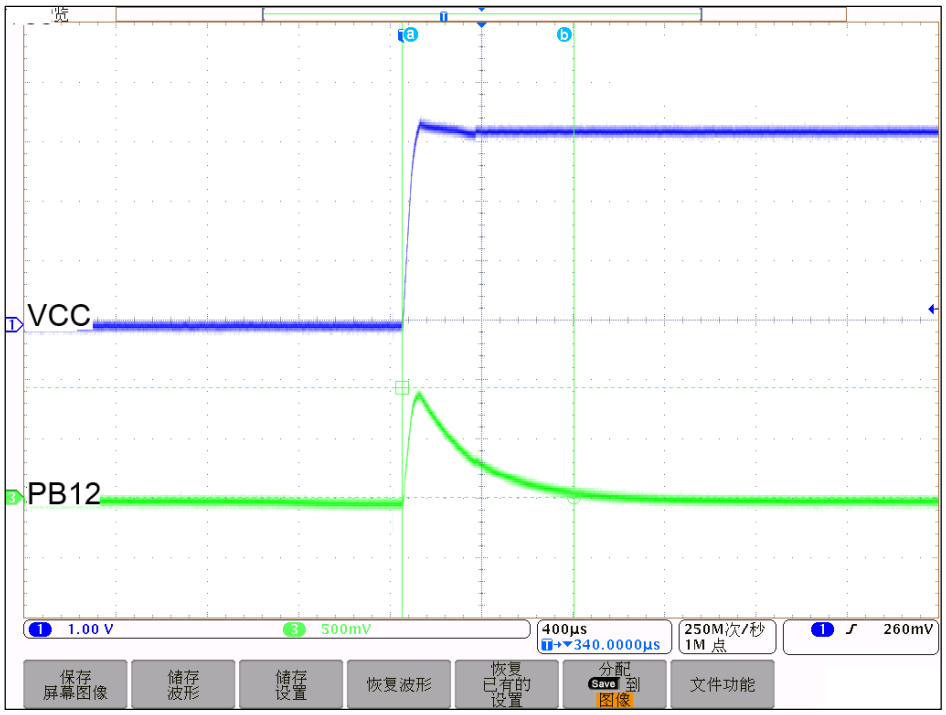

Figure 1-9 IO (PB12) waveform during power-on

The following figure shows the waveform of the development board N32H473CEU7_STB_V1.0 after adding a 10K pull-down resistor to IO (PB12) during power-on:

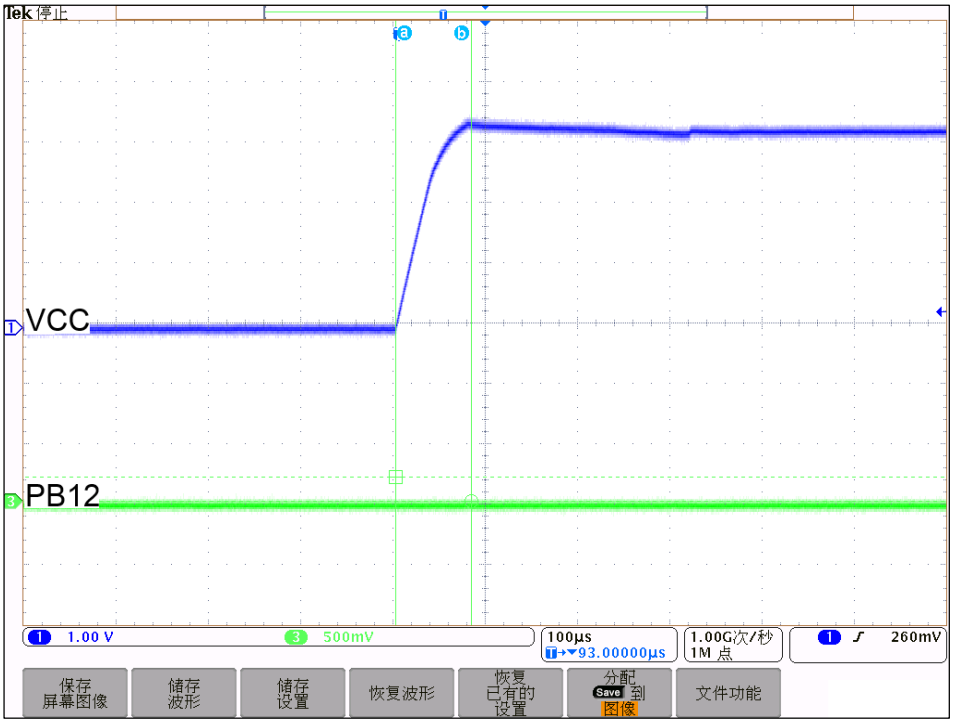

Figure 1-10 Waveform after IO (PB12) plus pull-down resistor during power-on process

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1.10 IO withstand voltage

Please pay attention to the withstand voltage value of each IO when using the chip. In the I/O structure column defined by pin multiplexing in the data sheet, FT: 5V tolerant IO is marked. This type of IO communicates with other external IOs in different voltage domains. , need to do level conversion.

Package									Pin Name	Type(1)	I / O Structure(2)	Fail-safe(3)	Main Function (After reset)	Pin Functions	
UQFN32	QFN48(4)	UQFN48	UQFN48-1	LQFP48	LQFP64	LQFP80	LQFP100	LQFP128						Alternate Functions	Additional Functions
-	-	-	-	-	-	-	1	1	PE2	I/O	FT	Yes	PE2	GTIM2_CH1 SPI4_SCK ATIM3_CH1 USART4_TX FEMC_A23 EVENTOUT	-
-	-	-	-	-	-	-	2	2	PE3	I/O	FT	Yes	PE3	GTIM2_CH2 SPI4_NSS ATIM3_CH2 USART4_RX FEMC_A19 EVENTOUT	-

Figure 1-11 I/O structure defined by pin multiplexing in the data sheet

Note: FT/FTa: 5V tolerant IO; TTa: 3.3V standard IO. When using the chip, you need to pay attention to the withstand voltage value of the IO.

1.11 Anti-static design

1.11.1 PCB Design

For the PCB design of ordinary two-layer boards, it is recommended that the signal lines be covered with ground, and the edges of the PCB board should be surrounded by ground as much as possible. If the cost allows, you can use a four-layer board or a multi-layer board design. In the multi-layer PCB, the ground plane acts as an important charge source, which can offset the charge on the electrostatic discharge source, which is beneficial to reducing the electrostatic field band. Come the question. The PCB ground plane can also serve as a shield for signal lines (of course, the larger the opening on the ground plane, the lower its shielding effectiveness). In addition, if a discharge occurs, due to the large ground plane of the PCB board, the charge is easily injected into the ground plane instead of entering the signal line. This will help protect the component because the charge can be discharged before causing damage to the component.

1.11.2 ESD Protection Devices

In actual product design, the chip itself has certain anti-static capabilities. The static electricity level in the N32H47X/N32H48X series MCU ESD (HBM) mode is +/-4KV. However, if there are higher ESD protection level requirements and there are chip management The pins need to be directly connected externally as the output or input port of the product. At this time, the pins of the chip are directly exposed to the outermost part of the product and

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cannot be isolated by laying the ground or other methods. Under such conditions, it is generally necessary to consider adding external ESD protection devices. TVS tubes are a typical ESD protection device. The following are examples of typical connection methods.

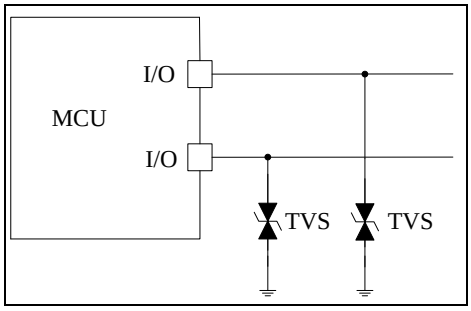

Figure 1-12 TVS connection on I/O pins

1.12 Debug Interface

N32H47X/N32H48X series chips support serial interface (SWD) and JTAG debug interface, please refer to the relevant user manual for detailed application.

Debug Signal	GPIO Pins
JTMS/SWDIO	PA13
JTCK/SWCLK	PA14
JTDI	PA15
JTDO	PB3
JNTRST	PB4

Table 1-1 Debug Interface

1.13 BOOT serial interface

N32H47X/N32H48X series chips support BOOT serial communication. The serial interface is as follows:

BOOT Serial Port	GPIO Pins
USART1_TX	PA9
USART1_RX	PA10

Table 1-2 Serial port interface

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2. Overall Design Suggestions

1） Printed circuit board

It is recommended to use a multi-layer printed circuit board with a dedicated independent ground plane (VSS) and a dedicated independent power supply plane (VDD), which can provide good coupling performance and shielding effect. In practical applications, if a multi-layer printed circuit board cannot be used considering the cost factor, a good grounding and power supply structure must be ensured when designing the circuit.

2） Component layout

In PCB design, different circuits need to be laid out separately according to the different effects of each device on EMI. For example, high-current circuits, low-voltage circuits, and digital devices. Thereby reducing cross-coupling on the PCB.

3） Power and ground (VDD, VSS)

Each module (noisy circuits, low-sensitivity circuits, digital circuits) should be grounded individually, and all grounds should eventually be connected together at one point. Try to avoid or reduce the area of the loop. In order to reduce the area of the power supply loop, the power supply should be as close as possible to the ground wire, because the power supply loop acts like an antenna and becomes an EMI transmitter and receiver. The area on the PCB without devices needs to be filled with ground to provide good shielding effect.

4） Decoupling

All power pins need to be properly connected to power. These connections, including pads, wires, and vias, should have as little impedance as possible. A common approach to increasing the trace width includes the use of separate power planes in multilayer PCBs. These capacitors should be placed as close as possible to the power/ground pins. The figure below shows a typical layout of such a power/ground pin.

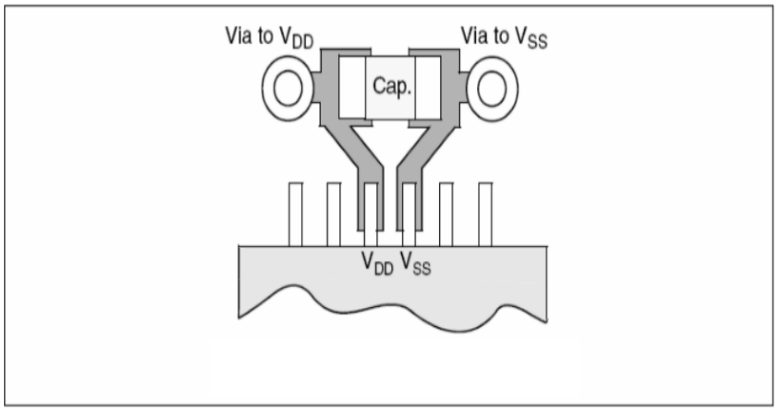

Figure 2-1 Typical layout of VDD/VSS pins

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3. Minimum System Reference Design Schematic

3.1 UQFN32-N32H473KEU7

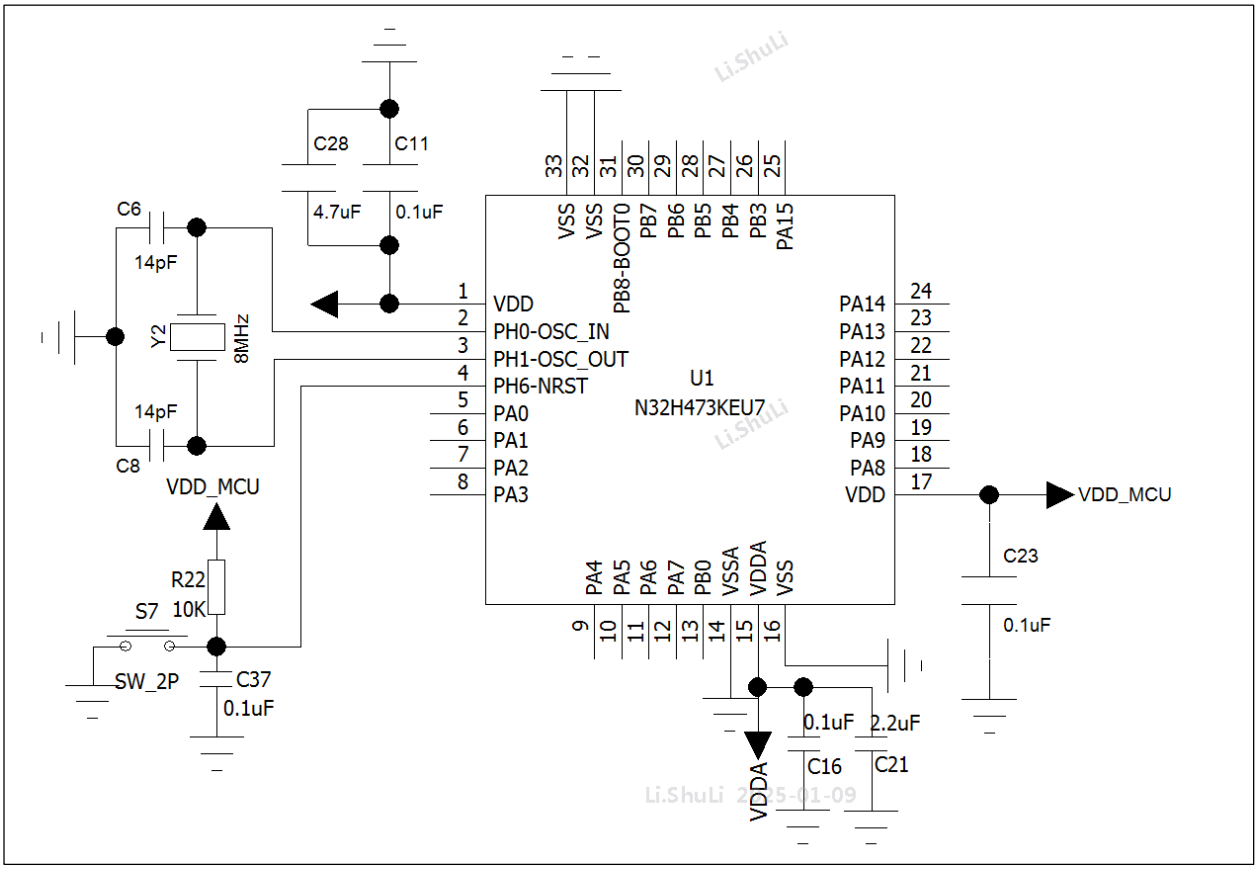

Figure 3-1 UQFN32 minimum package system reference design schematic diagram

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3.2 LQFP48-N32H473CEL7

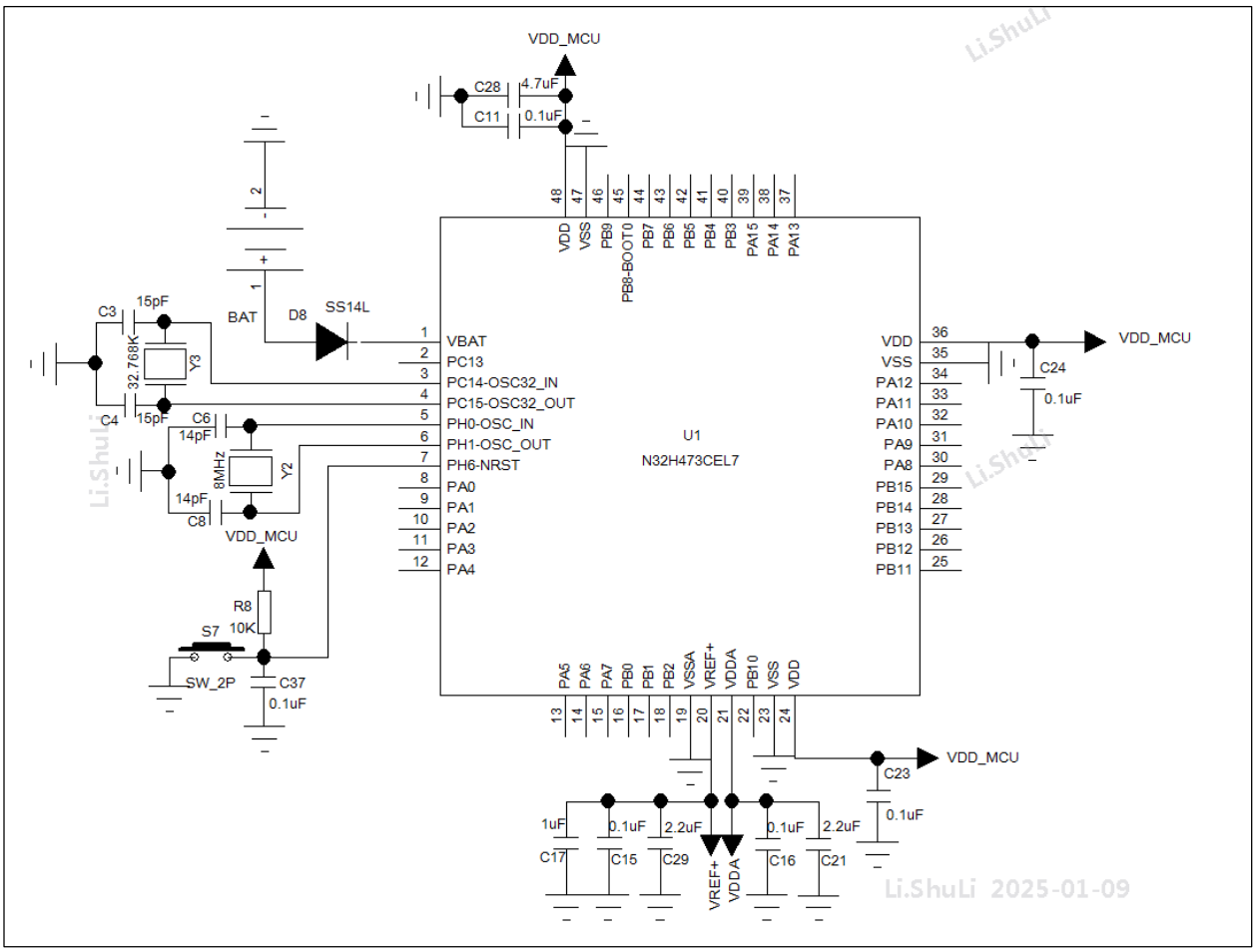

Figure 3-2 LQFP48 minimum package system reference design schematic diagram

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3.3 LQFP48-N32H474CEL7

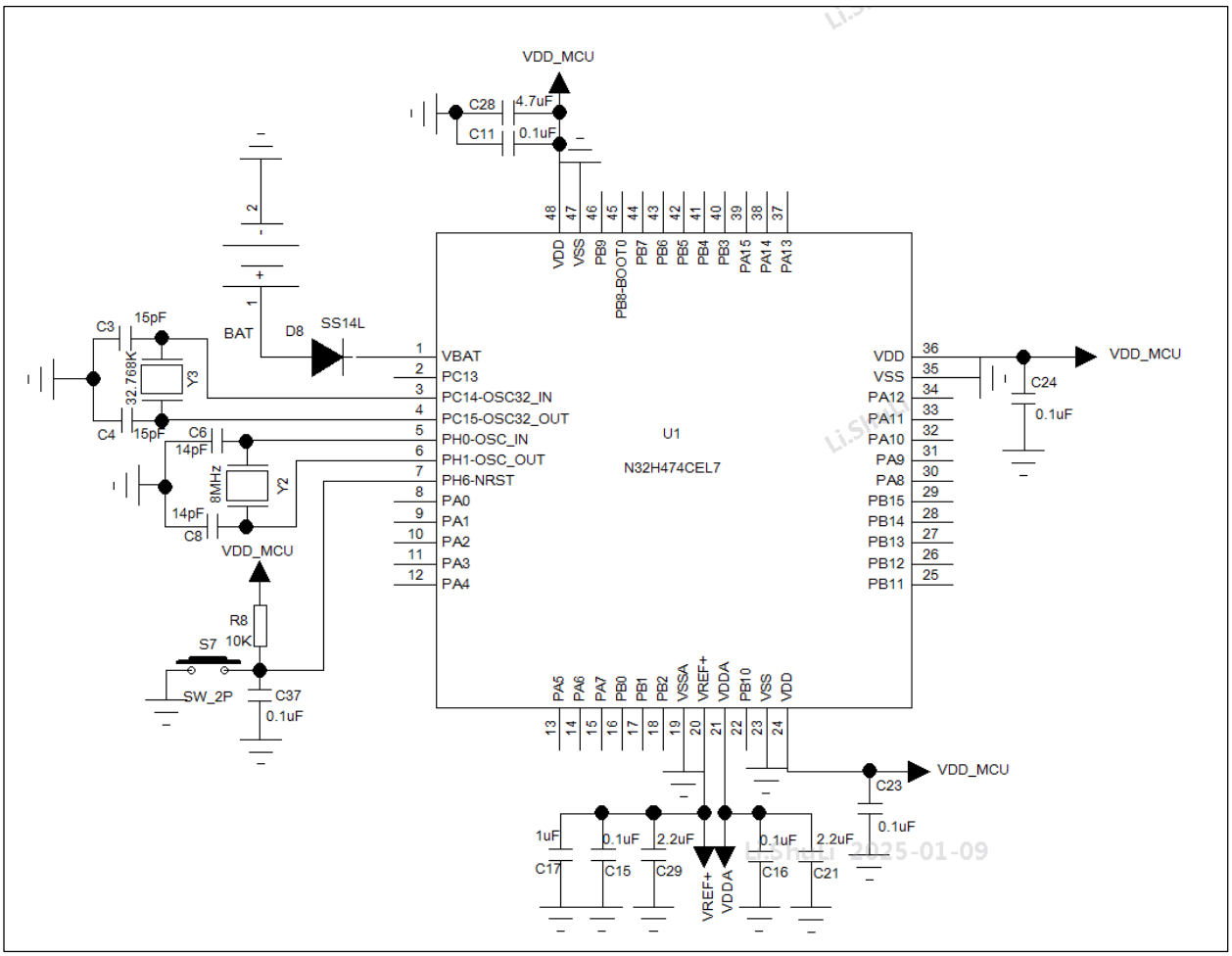

Figure 3-3 LQFP48 minimum package system reference design schematic diagram

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3.4 QFN48-N32H473CGQ8

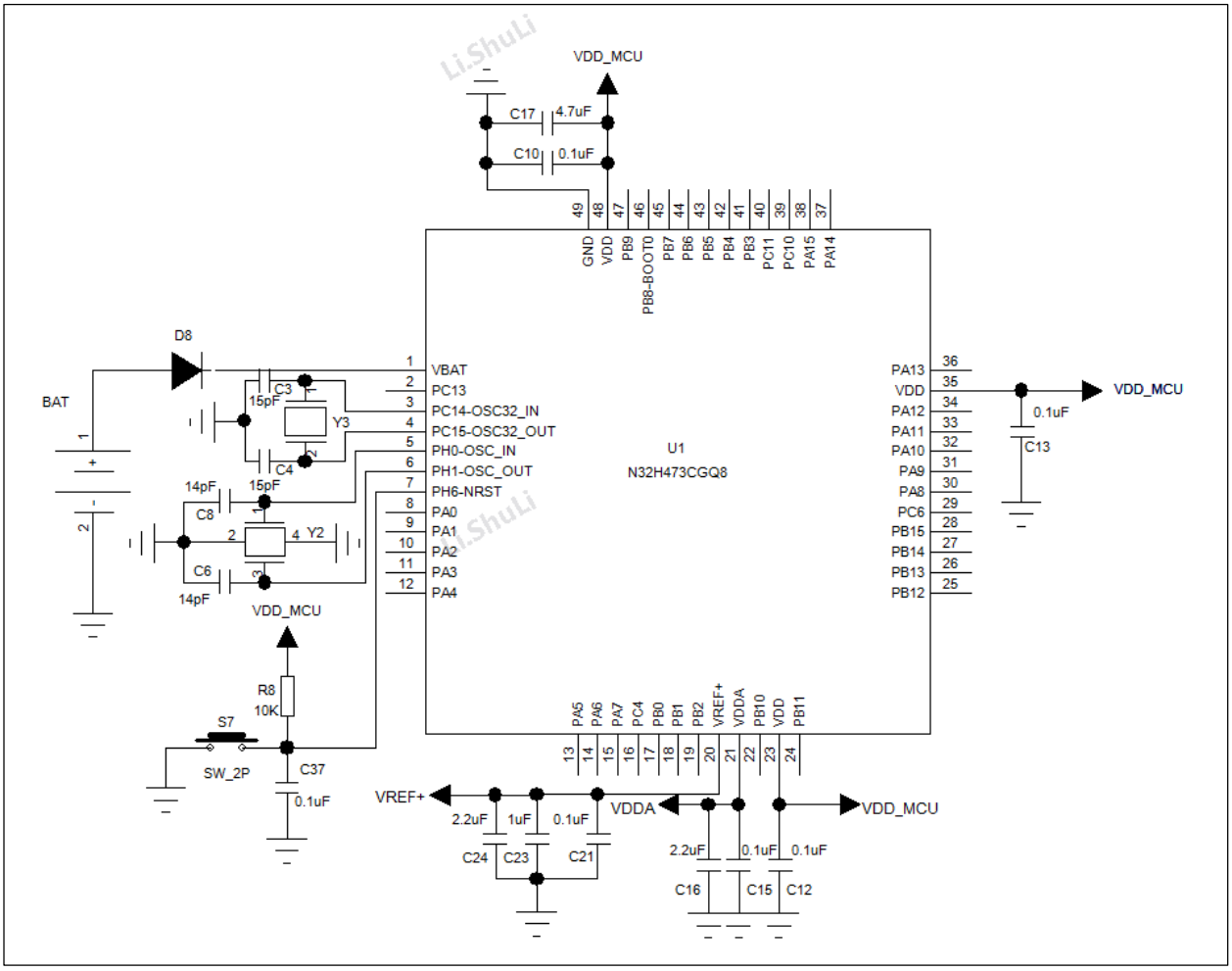

Figure 3-4 QFN48 minimum package system reference design schematic diagram

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3.5 UQFN48-N32H473CEU7

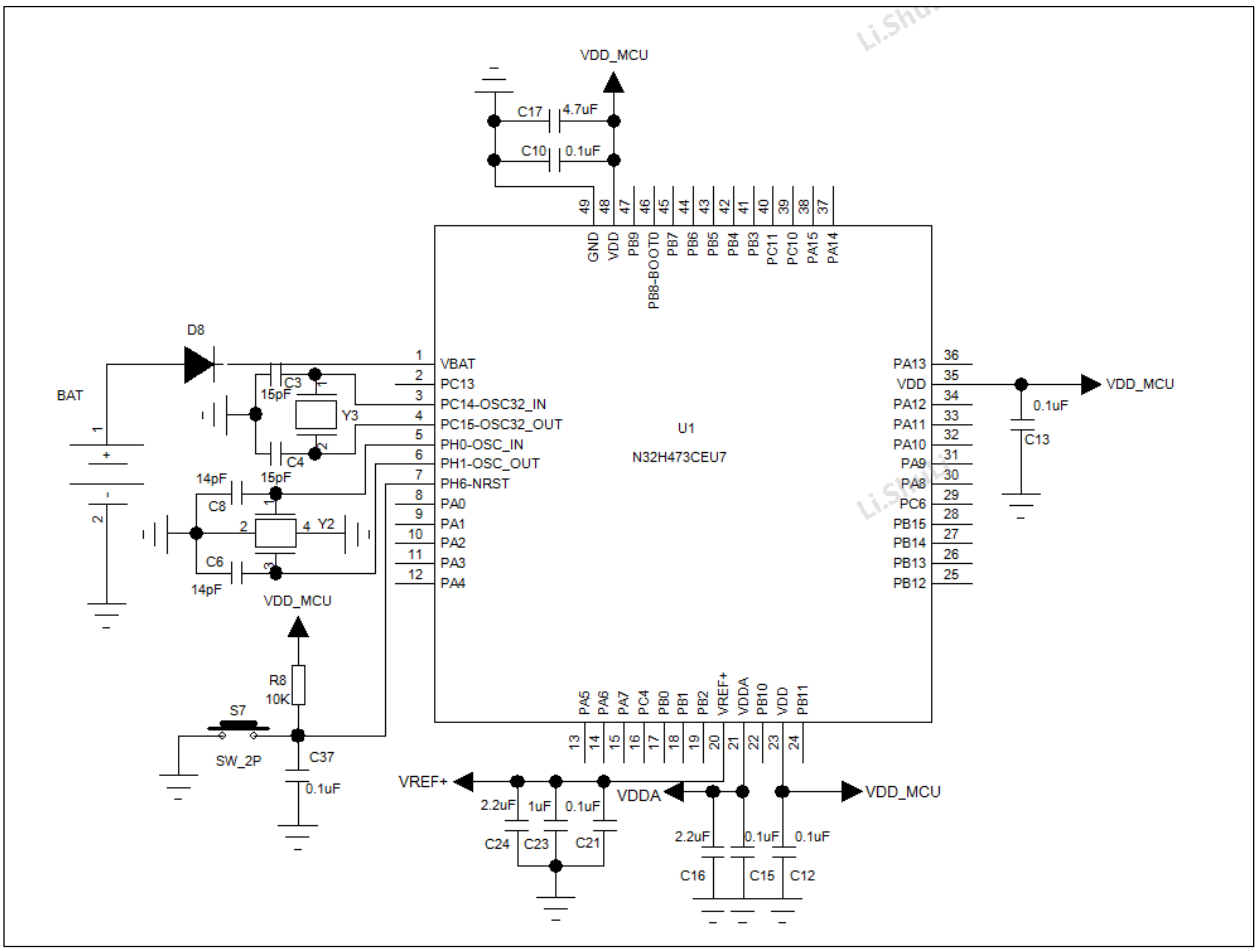

Figure 3-5 UQFN48 minimum package system reference design schematic diagram

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3.6 UQFN48-1-N32H473CCU7E

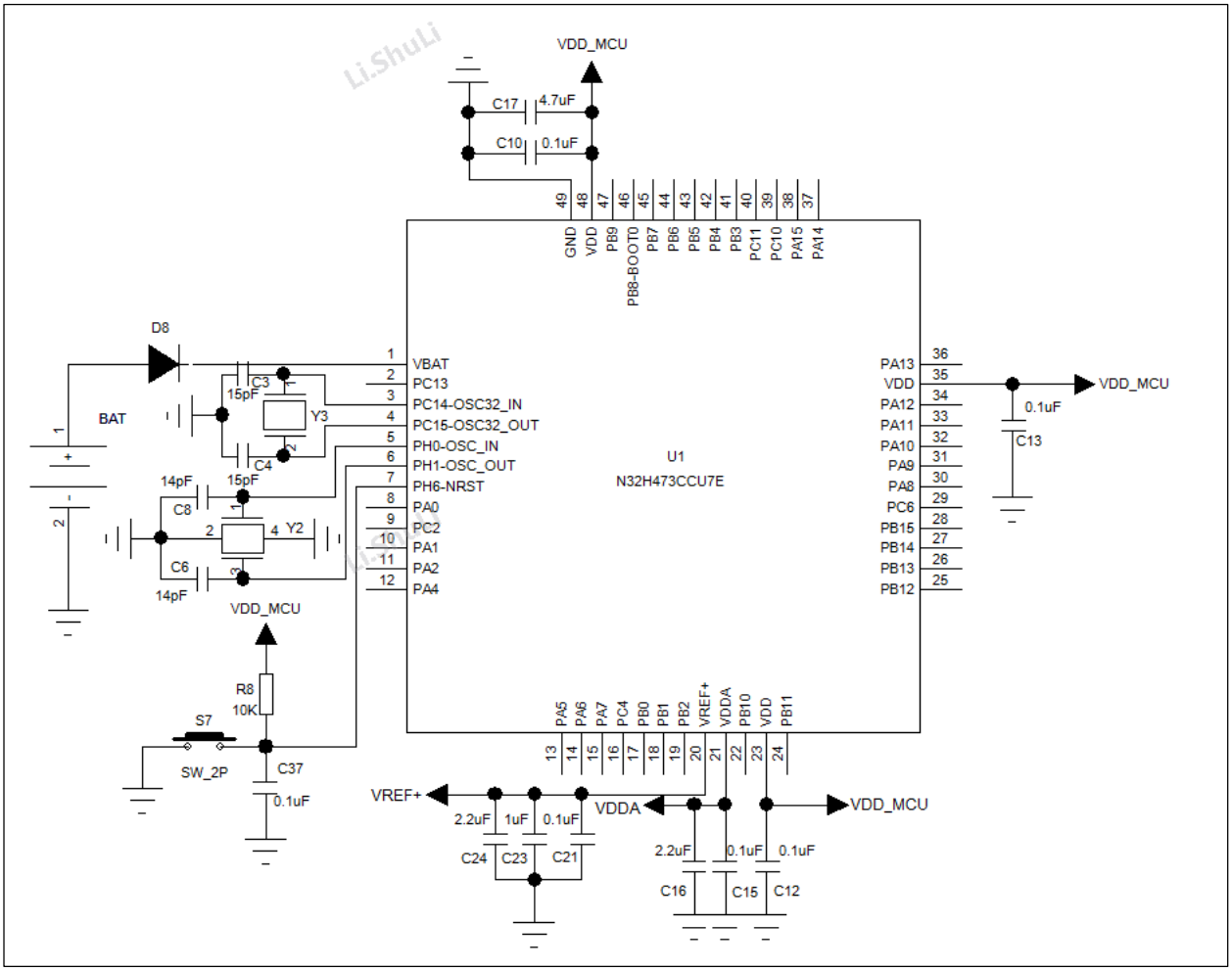

Figure 3-6 UQFN48-1 minimum package system reference design schematic diagram

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3.7 UQFN48-N32H474CEU7

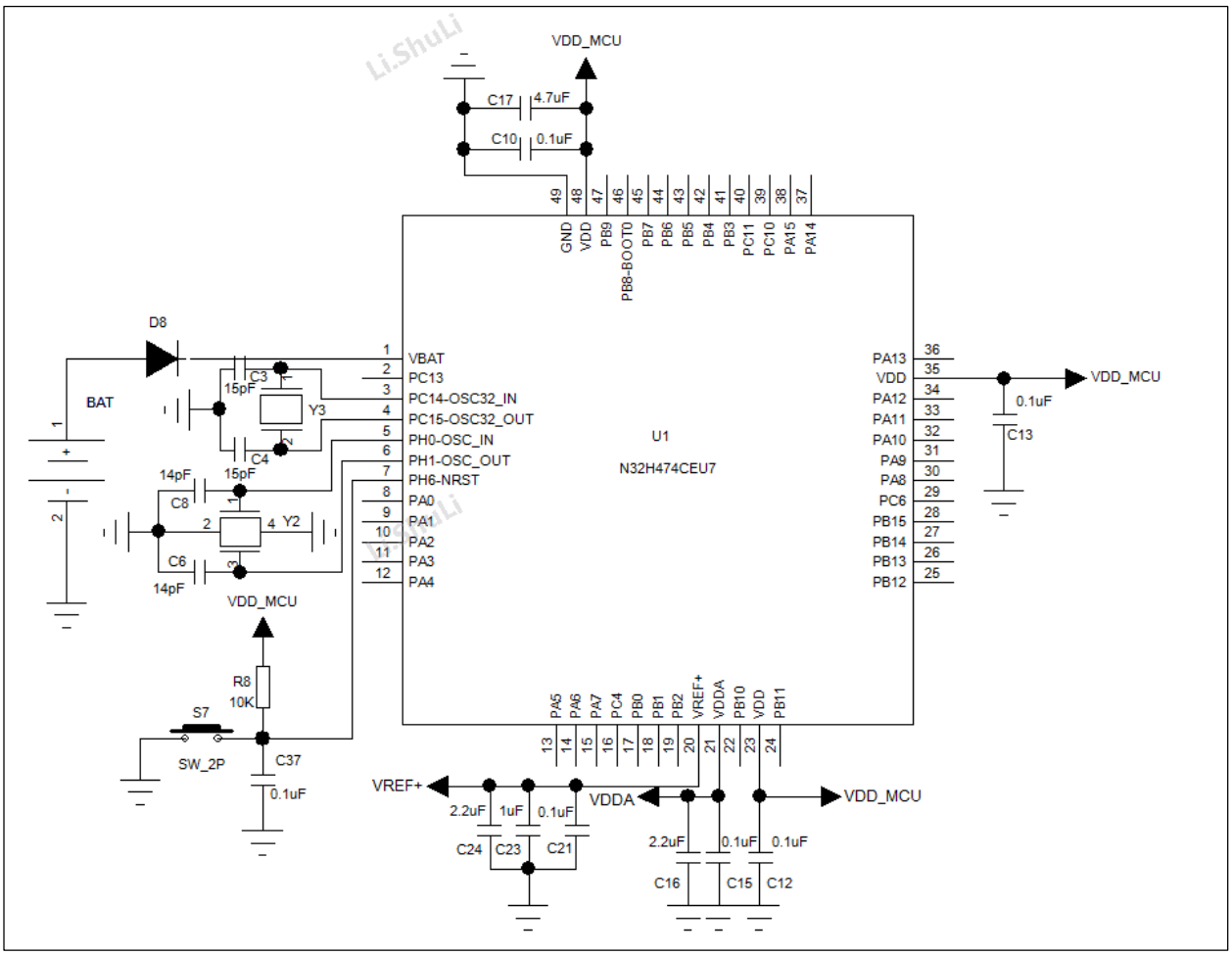

Figure 3-7 UQFN48 minimum package system reference design schematic diagram

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3.8 QFN52-N32H475UEQ7S

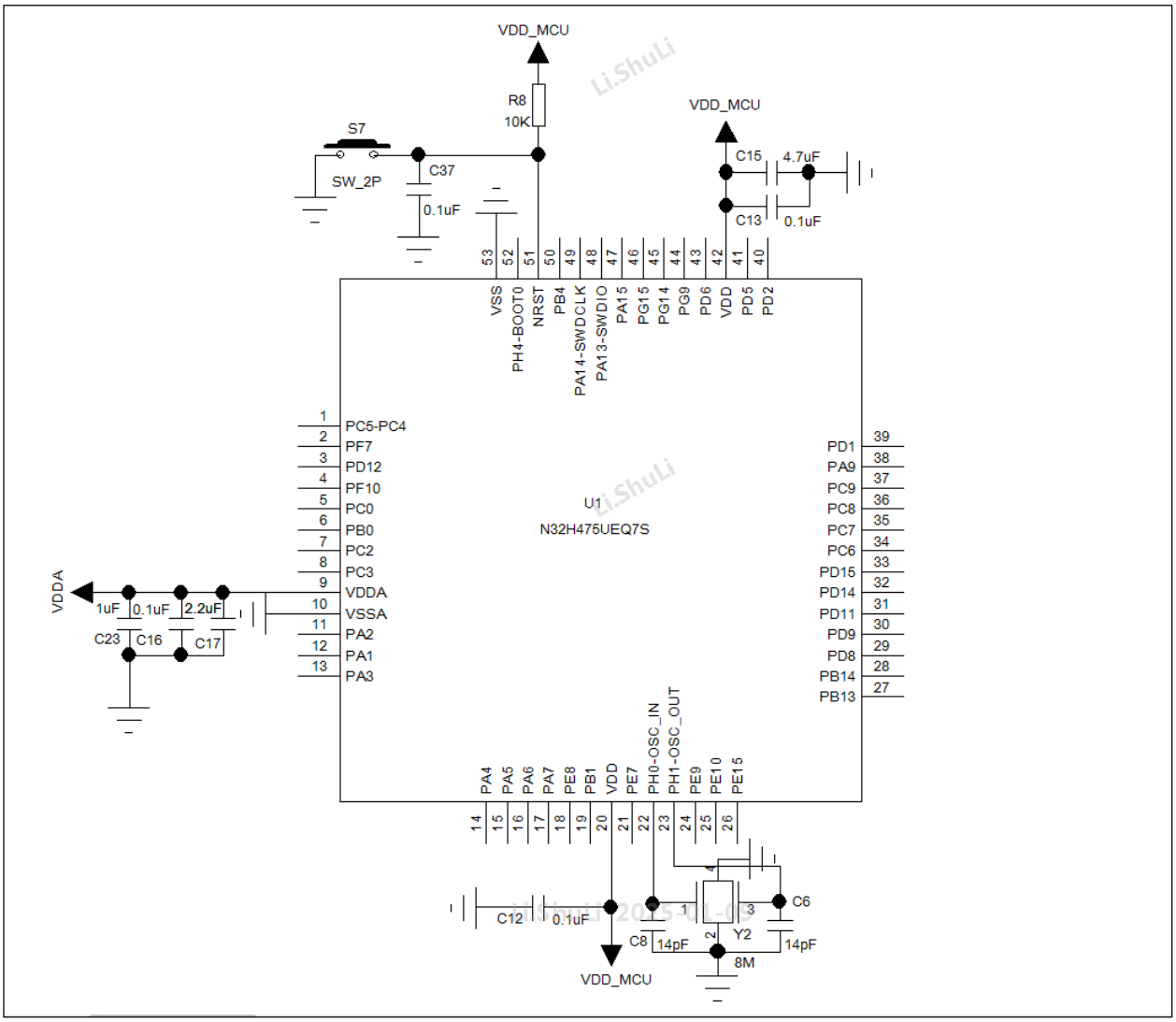

Figure 3-8 QFN52 minimum package system reference design schematic diagram

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3.9 QFN60-N32H475REQ7

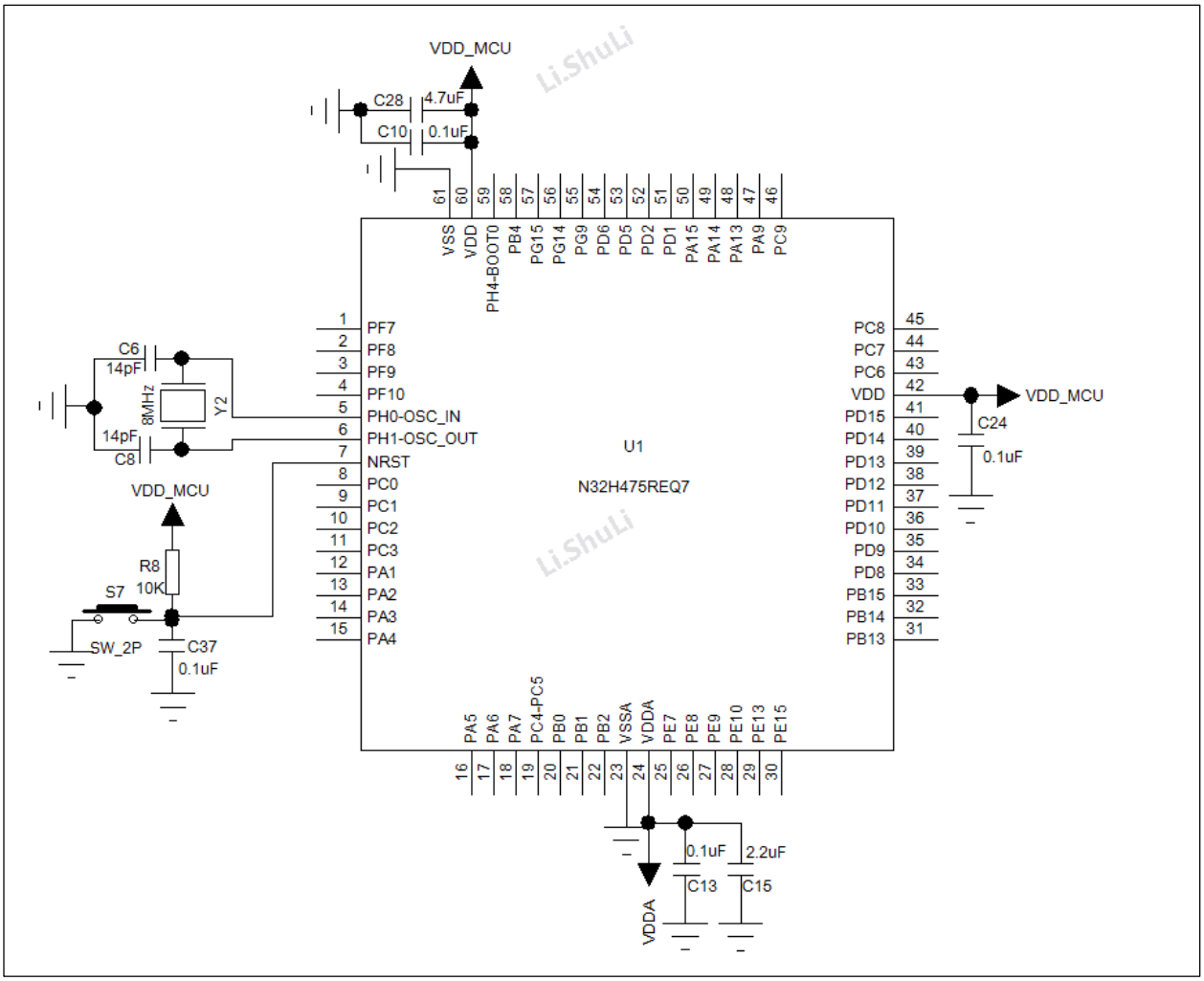

Figure 3-9 QFN60 minimum package system reference design schematic diagram

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3.10 LQFP64-N32H473REL7

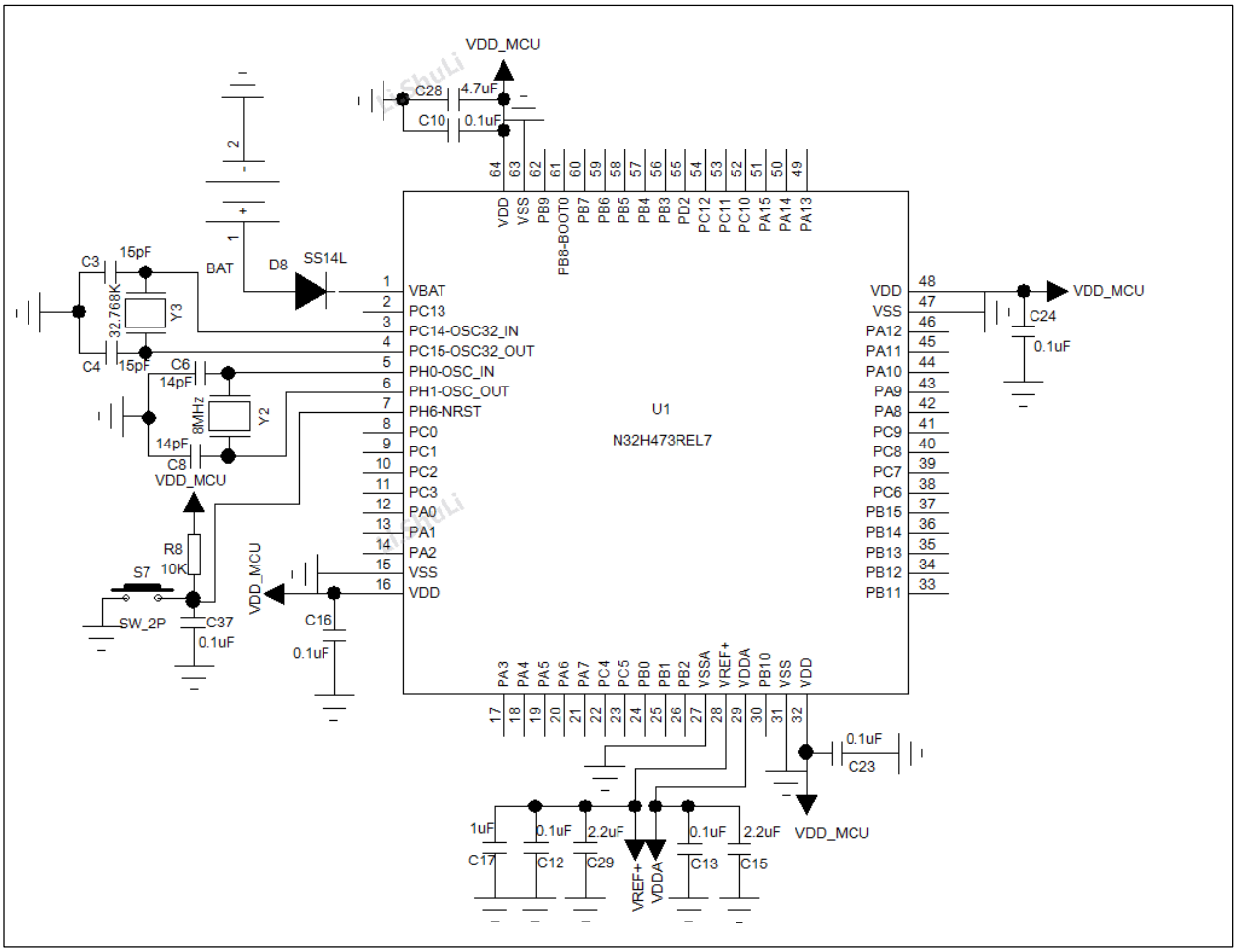

Figure 3-10 LQFP64 minimum package system reference design schematic diagram

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3.11 LQFP64-N32H474REL7

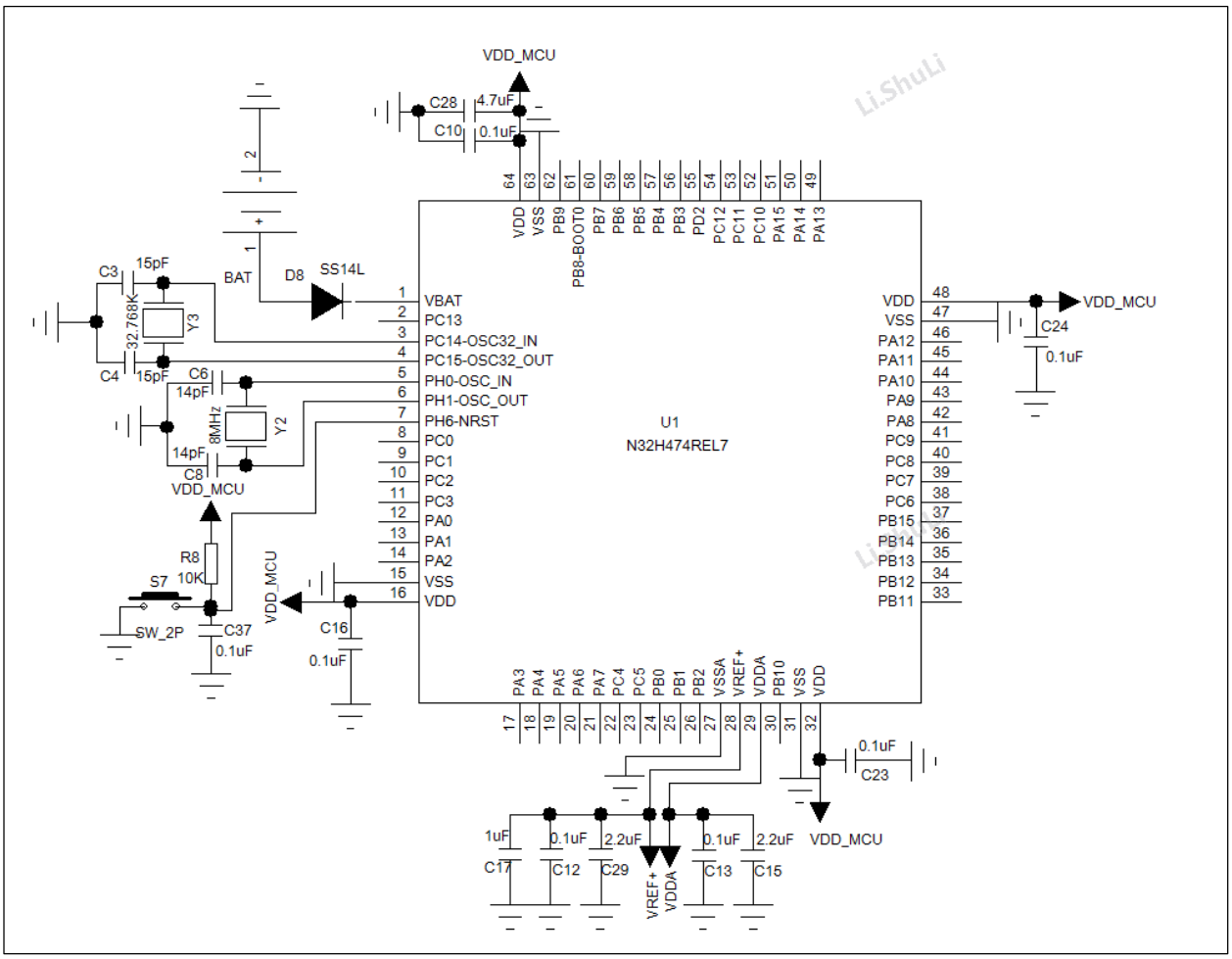

Figure 3-11 LQFP64 minimum package system reference design schematic diagram

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3.12 LQFP64-N32H481REL7K

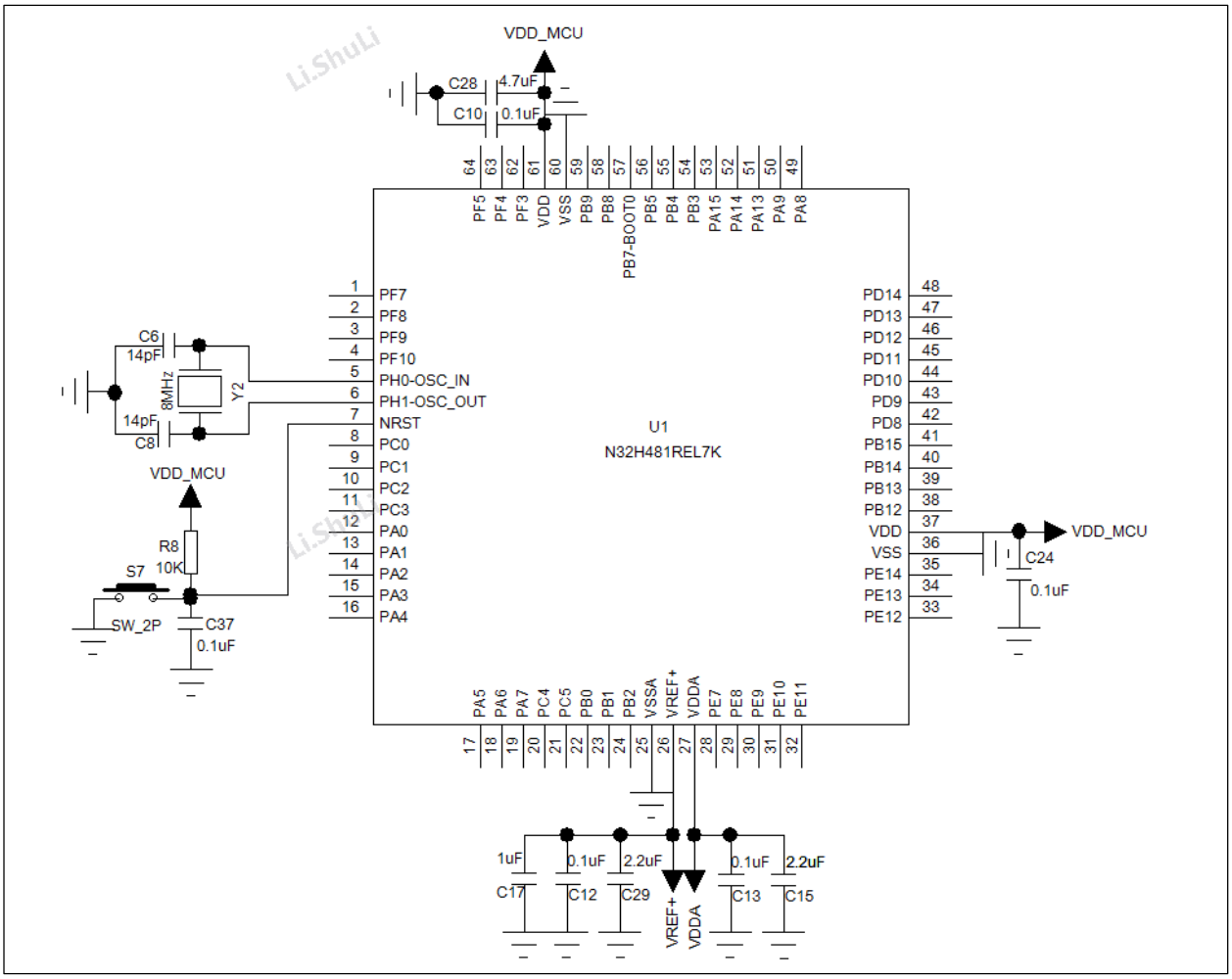

Figure 3-12 LQFP64 minimum package system reference design schematic diagram

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3.13 LQFP64-N32H488REL7K

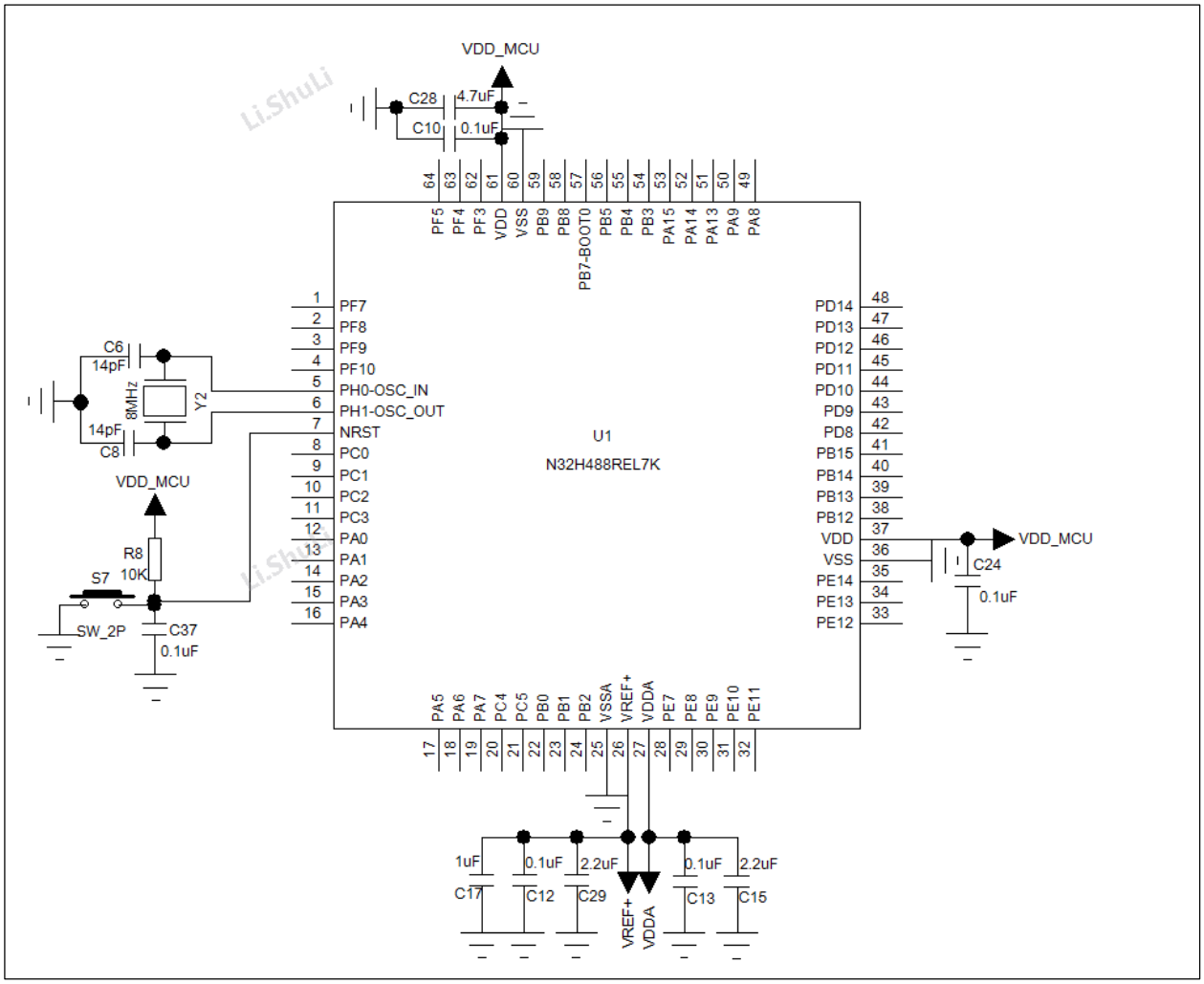

Figure 3-13 LQFP64 minimum package system reference design schematic diagram

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3.14 LQFP64-N32H482REL7

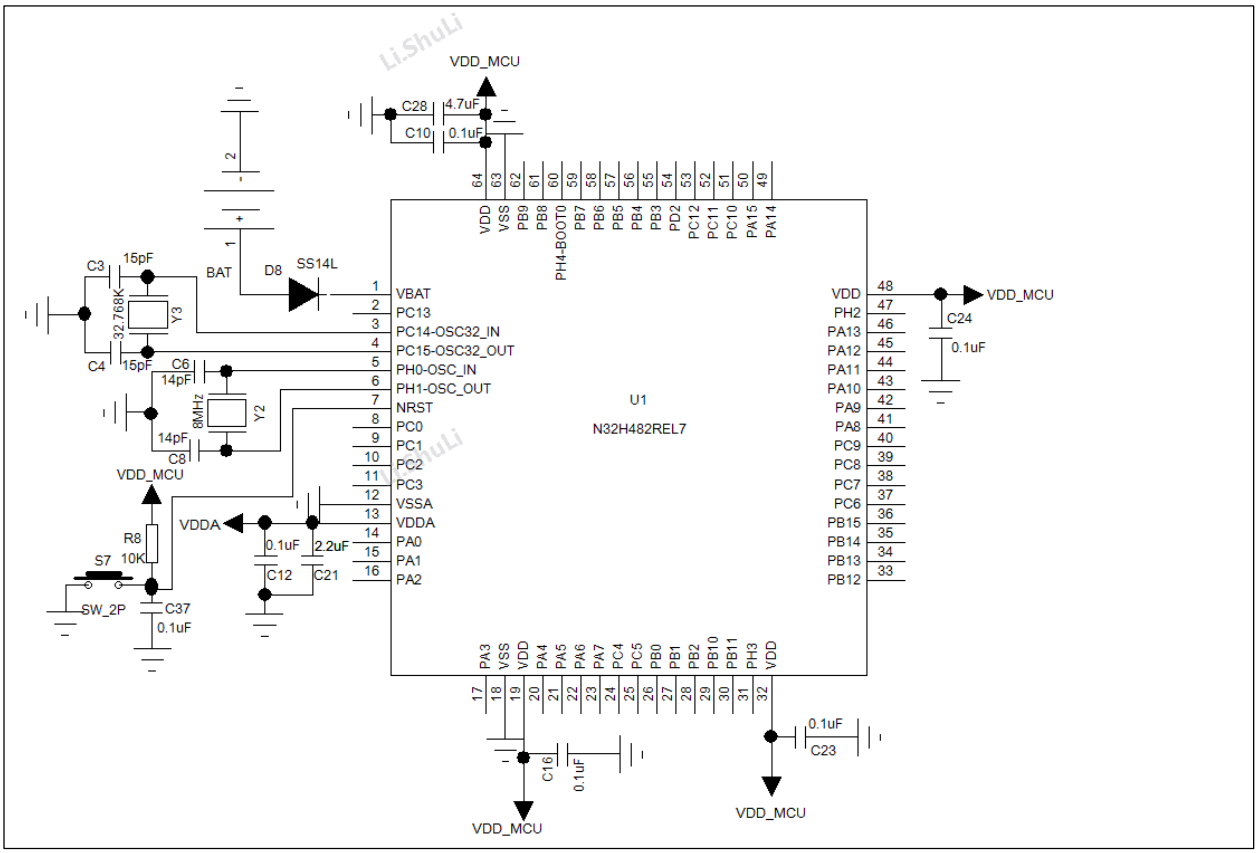

Figure 3-14 LQFP64 minimum package system reference design schematic diagram

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3.15 LQFP64-N32H487REL7

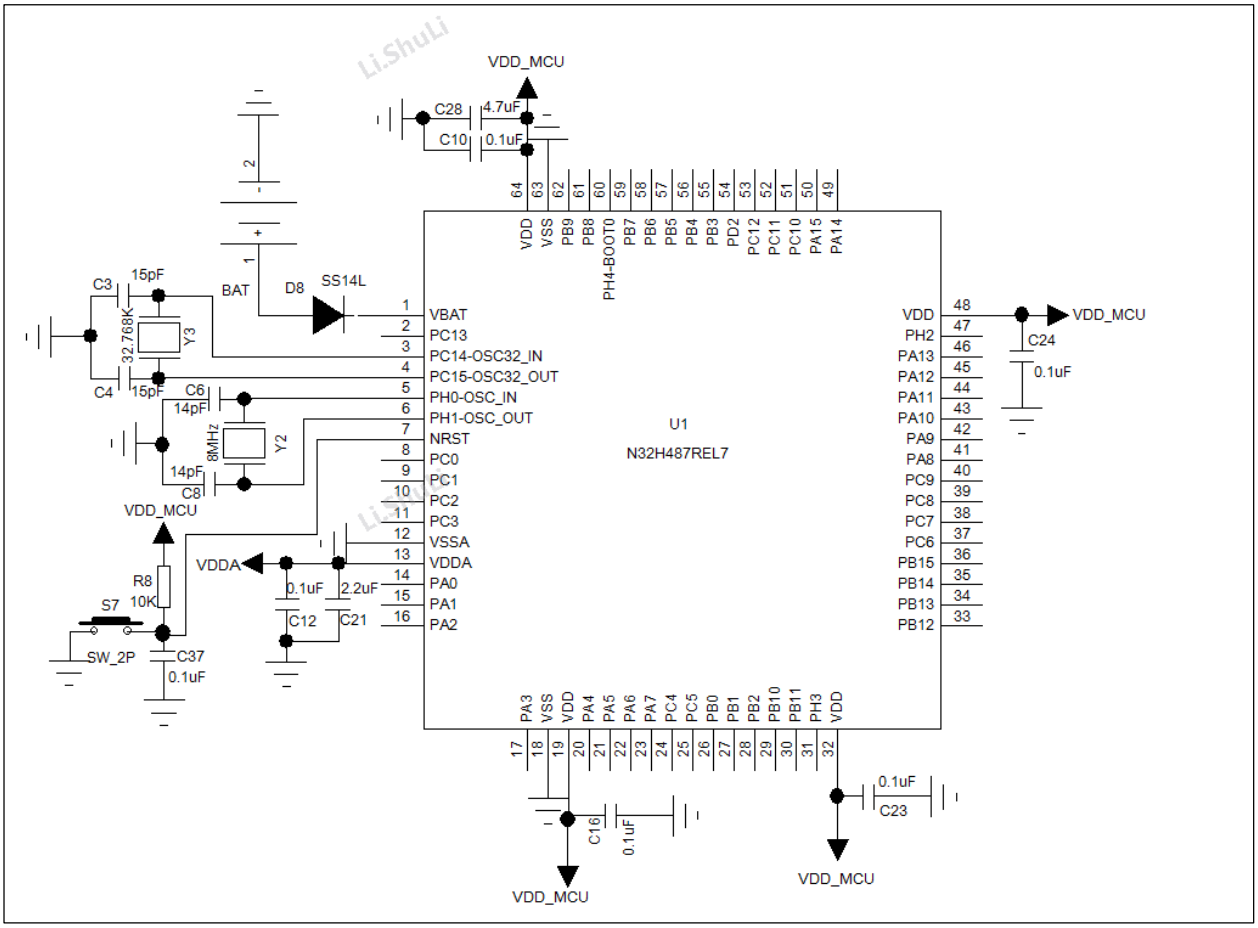

Figure 3-15 LQFP64 minimum package system reference design schematic diagram

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3.16 LQFP64-N32H488REL7

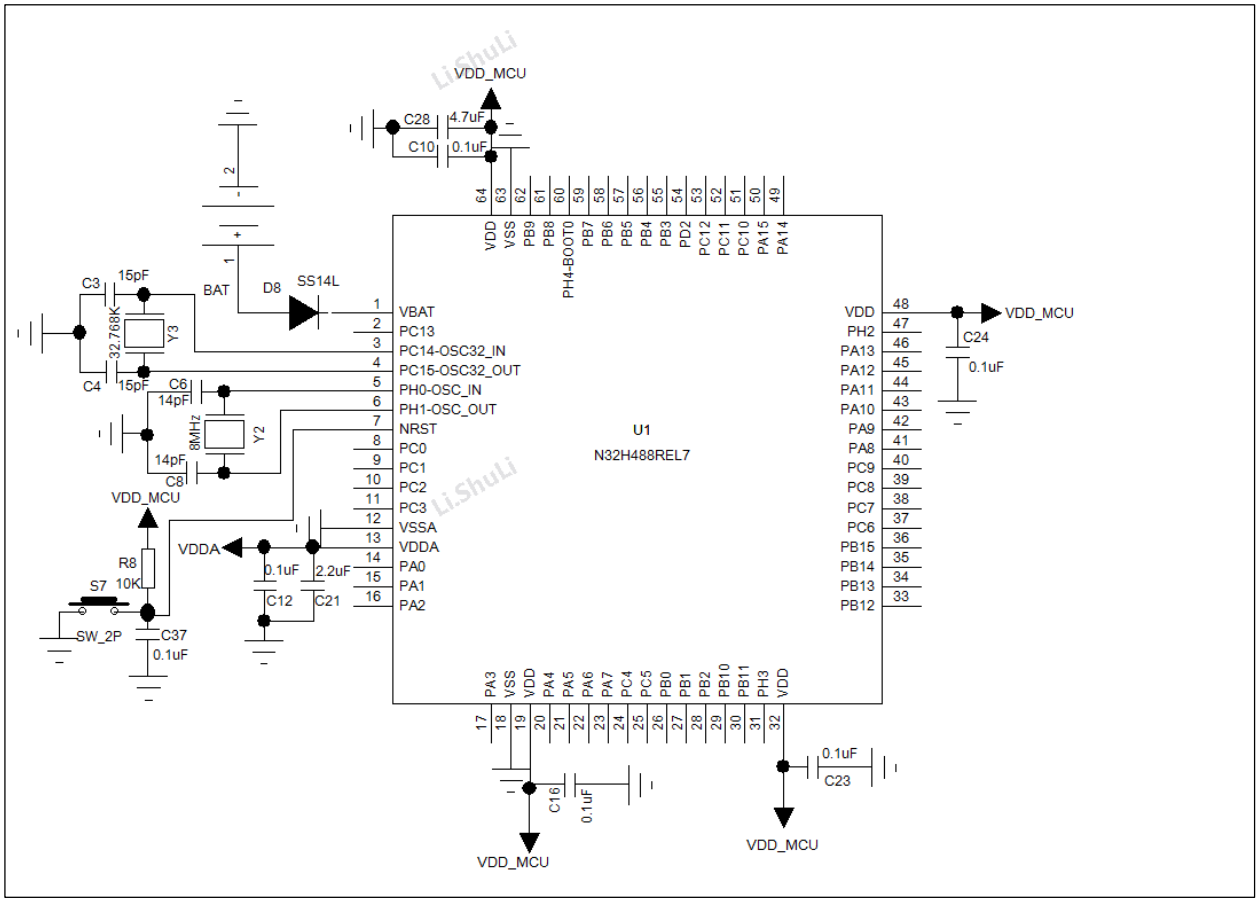

Figure 3-16 LQFP64 minimum package system reference design schematic diagram

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3.17 LQFP80-N32H473MEL7

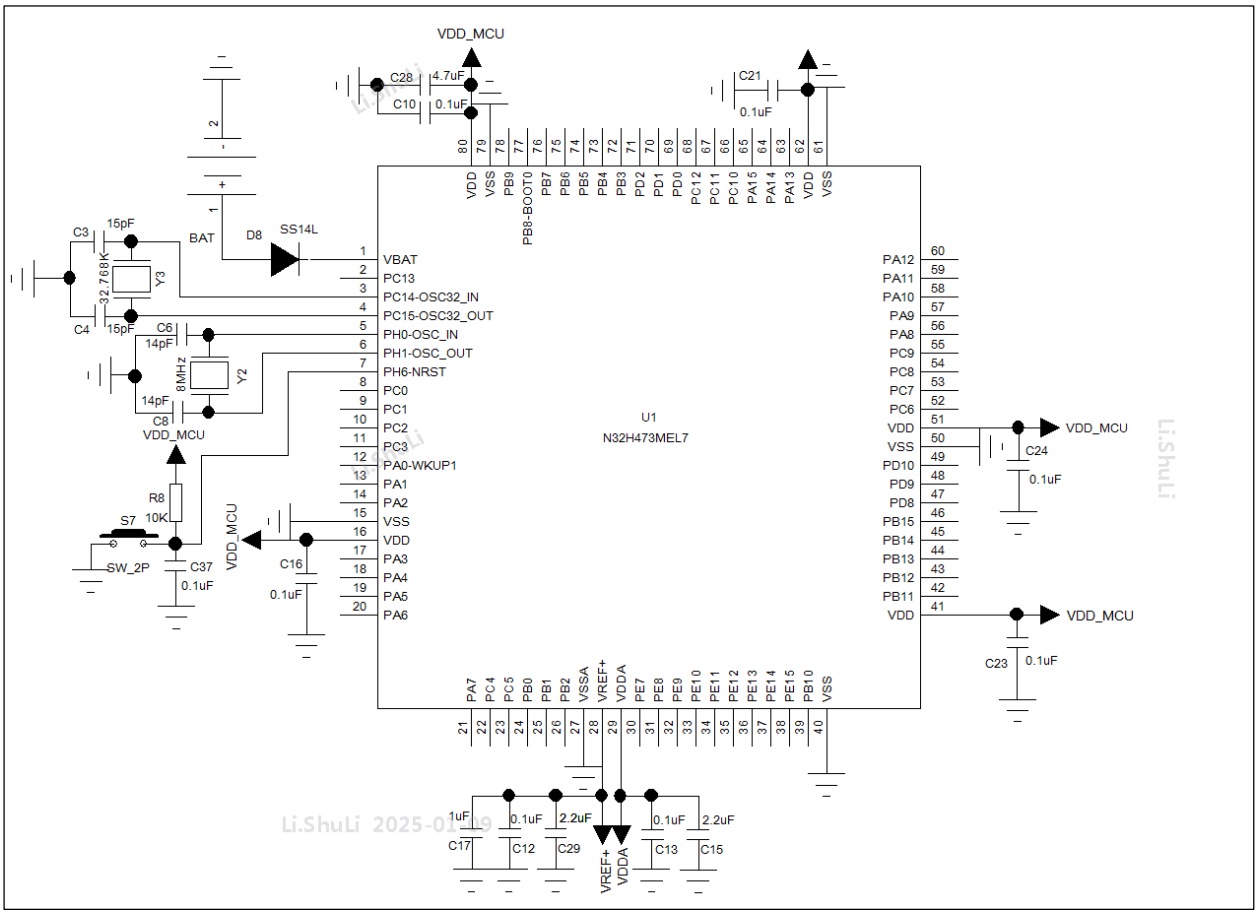

Figure 3-17 LQFP80 minimum package system reference design schematic diagram

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3.18 LQFP80-N32H474MEL7

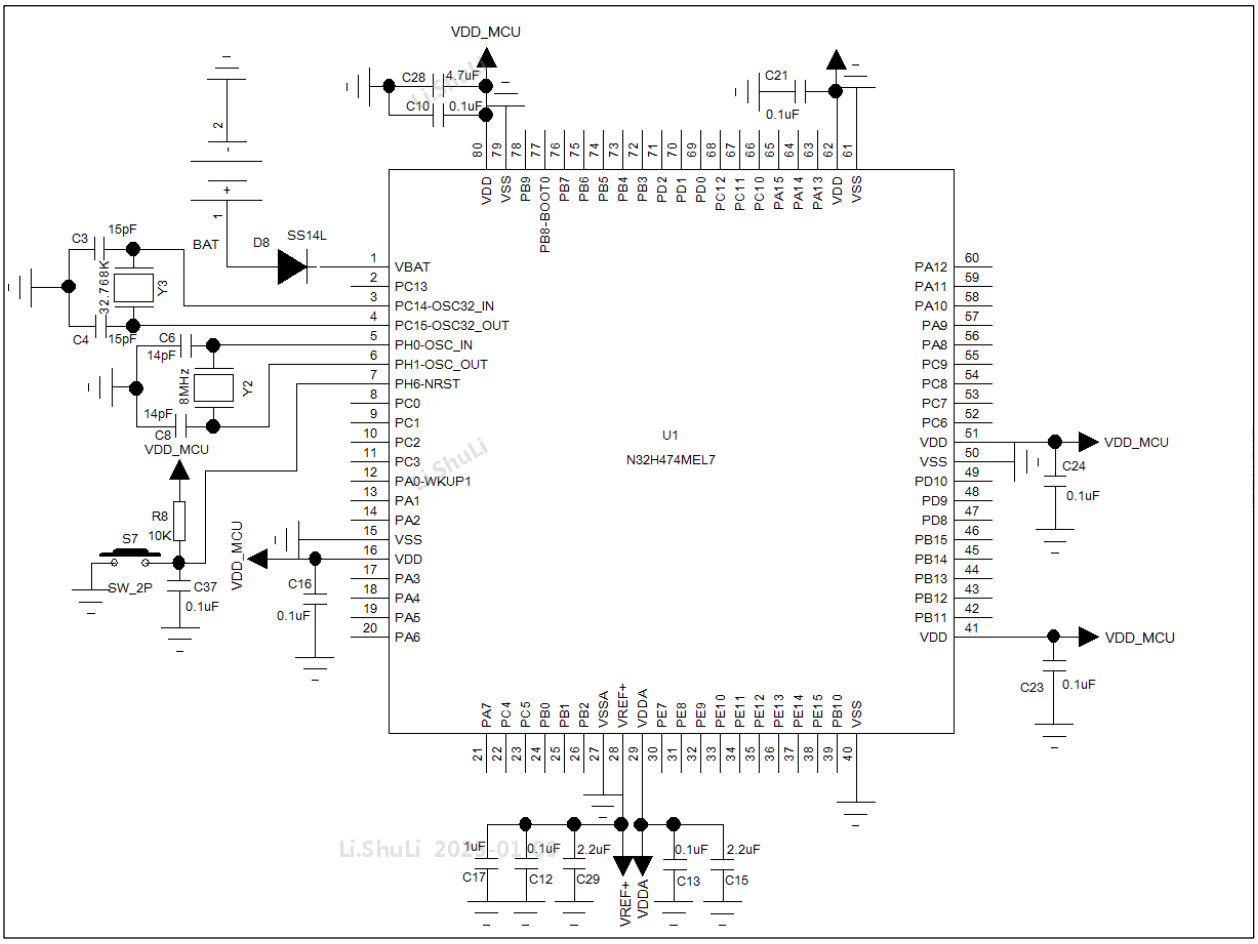

Figure 3-18 LQFP80 minimum package system reference design schematic diagram

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3.19 LQFP100-N32H474VEL7

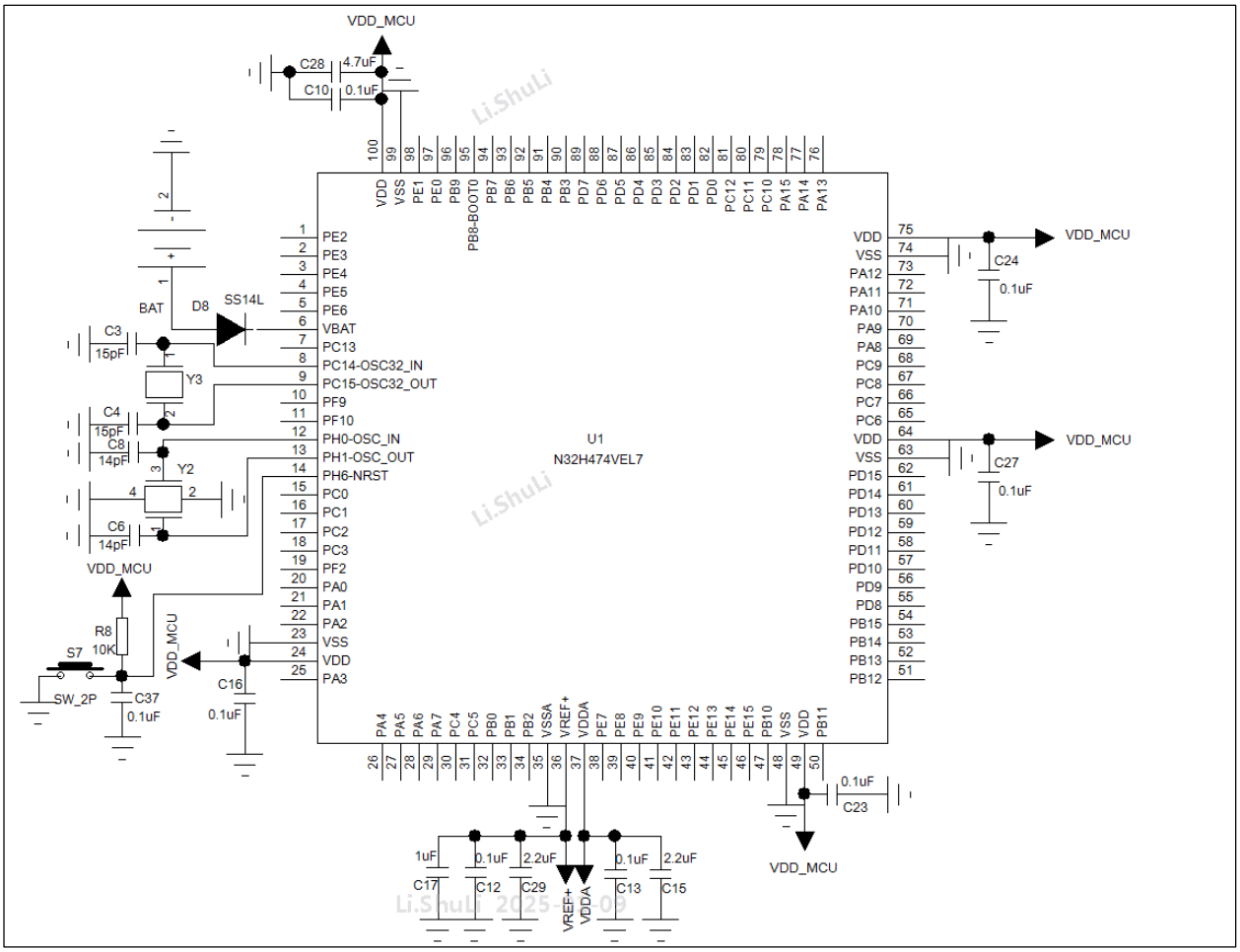

Figure 3-19 LQFP100 minimum package system reference design schematic diagram

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3.20 LQFP100-N32H473VEL7

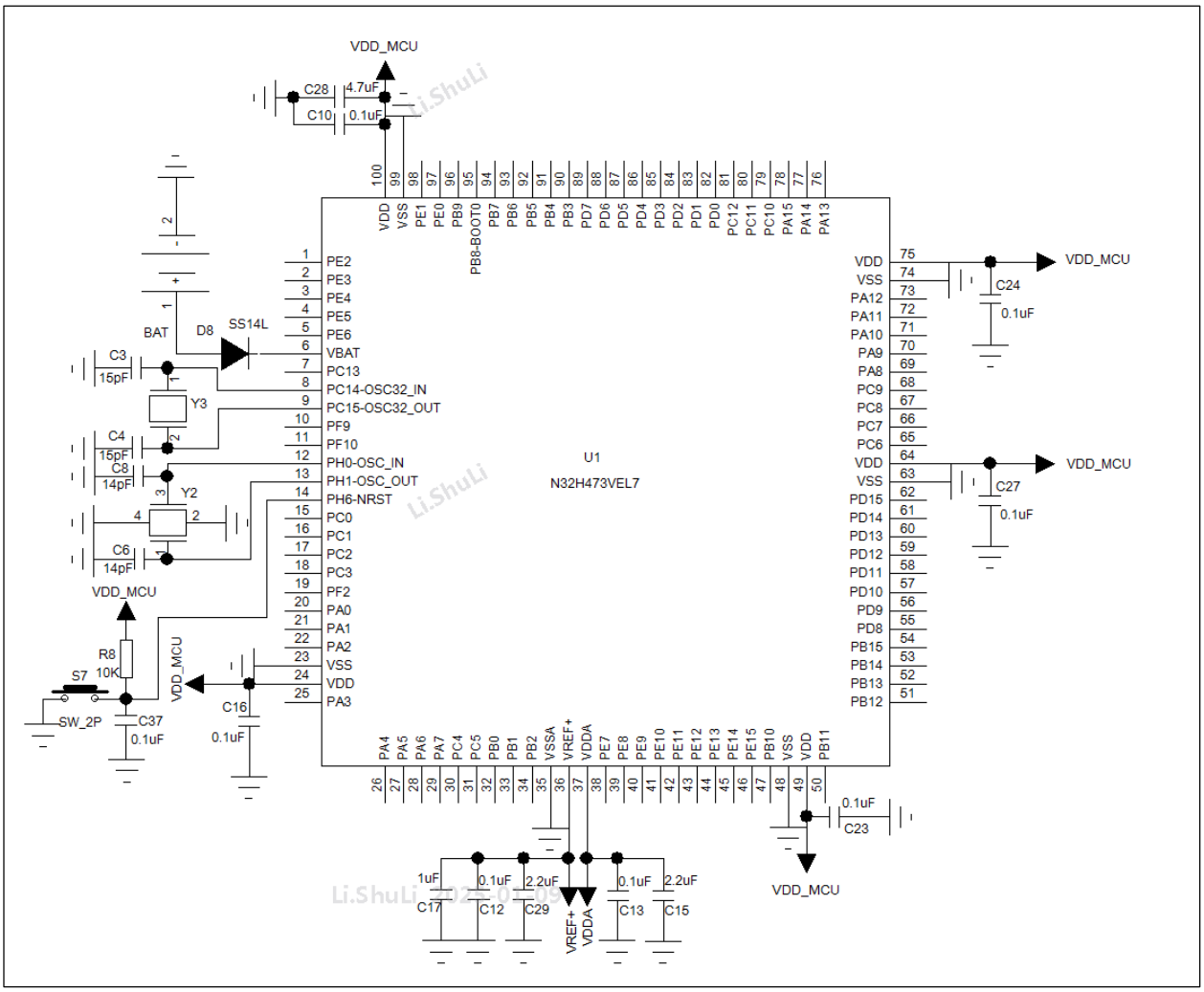

Figure 3-20 LQFP100 minimum package system reference design schematic diagram

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3.21 LQFP100-N32H482VEL7

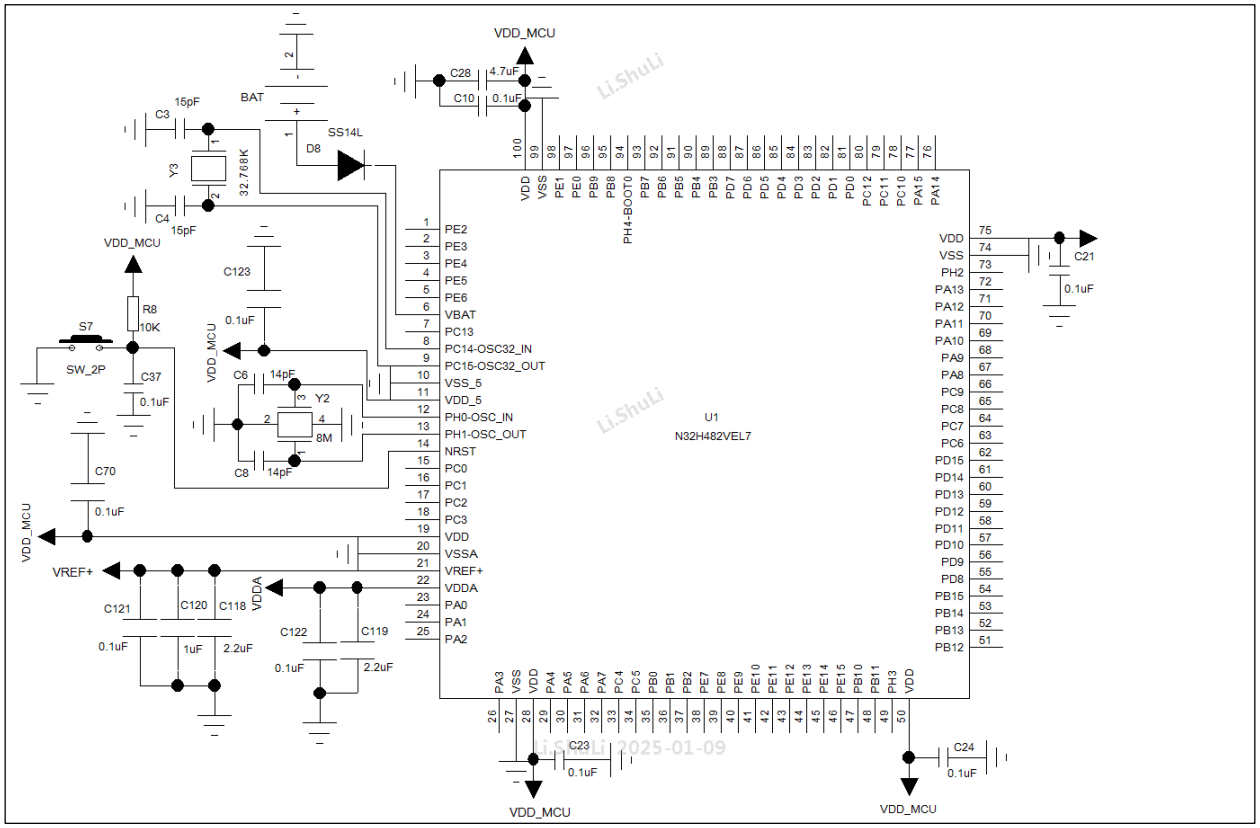

Figure 3-21 LQFP100 minimum package system reference design schematic diagram

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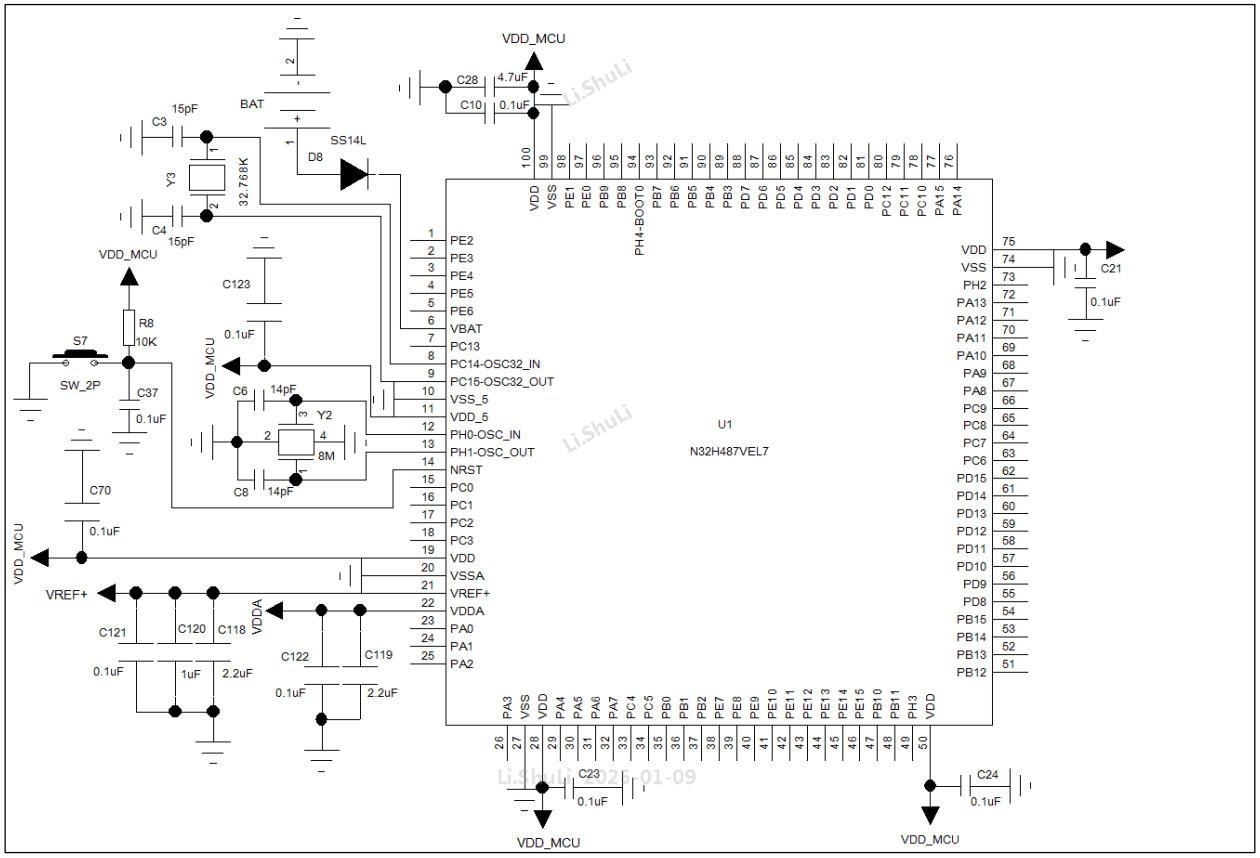
3.22 LQFP100-N32H487VEL7



图

Figure 3-22 LQFP100 minimum package system reference design schematic diagram

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3.23 LQFP100-N32H488VEL7

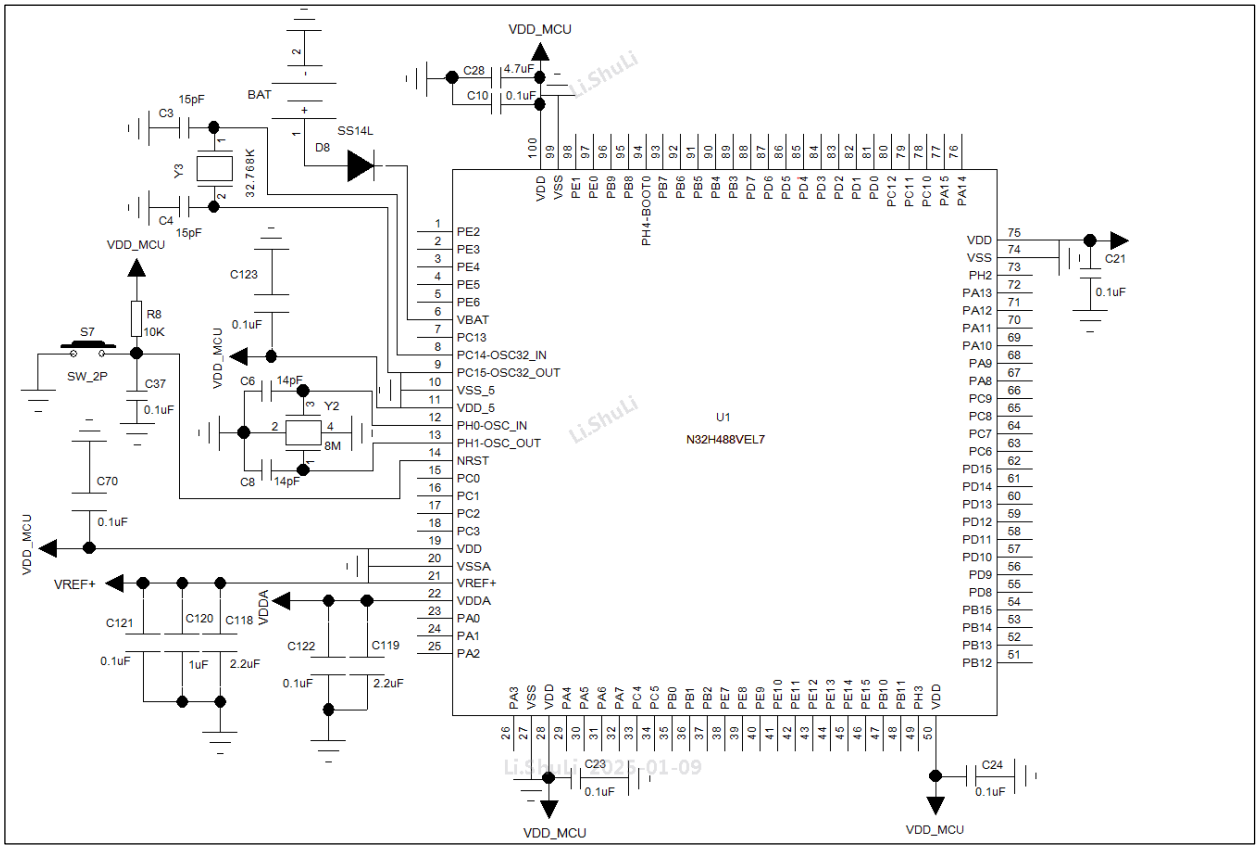

Figure 3-23 LQFP100 minimum package system reference design schematic diagram

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3.24 LQFP128-N32H474QEL7

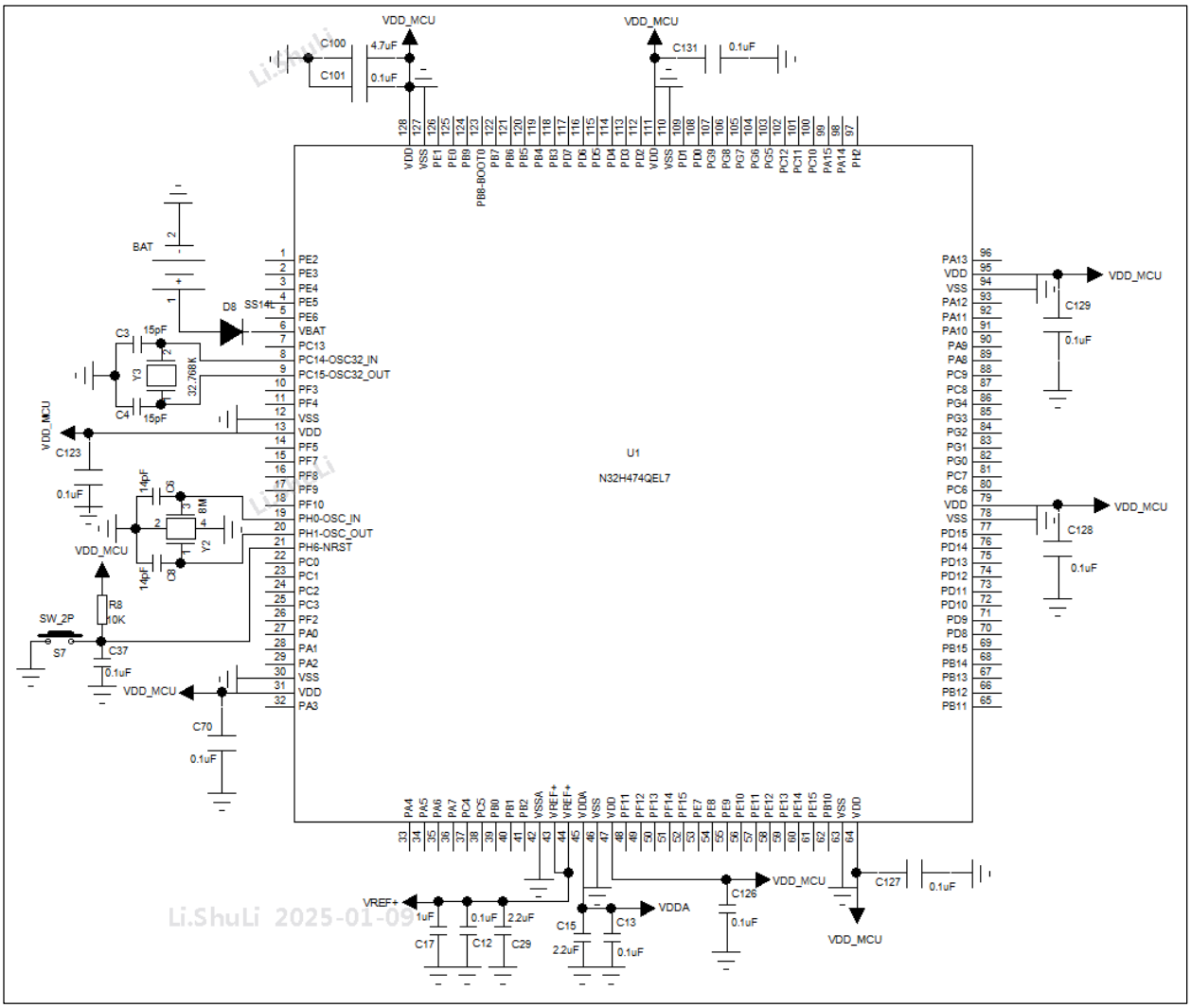

Figure 3-24 LQFP128 minimum package system reference design schematic diagram

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3.25 LQFP128-N32H473QEL7

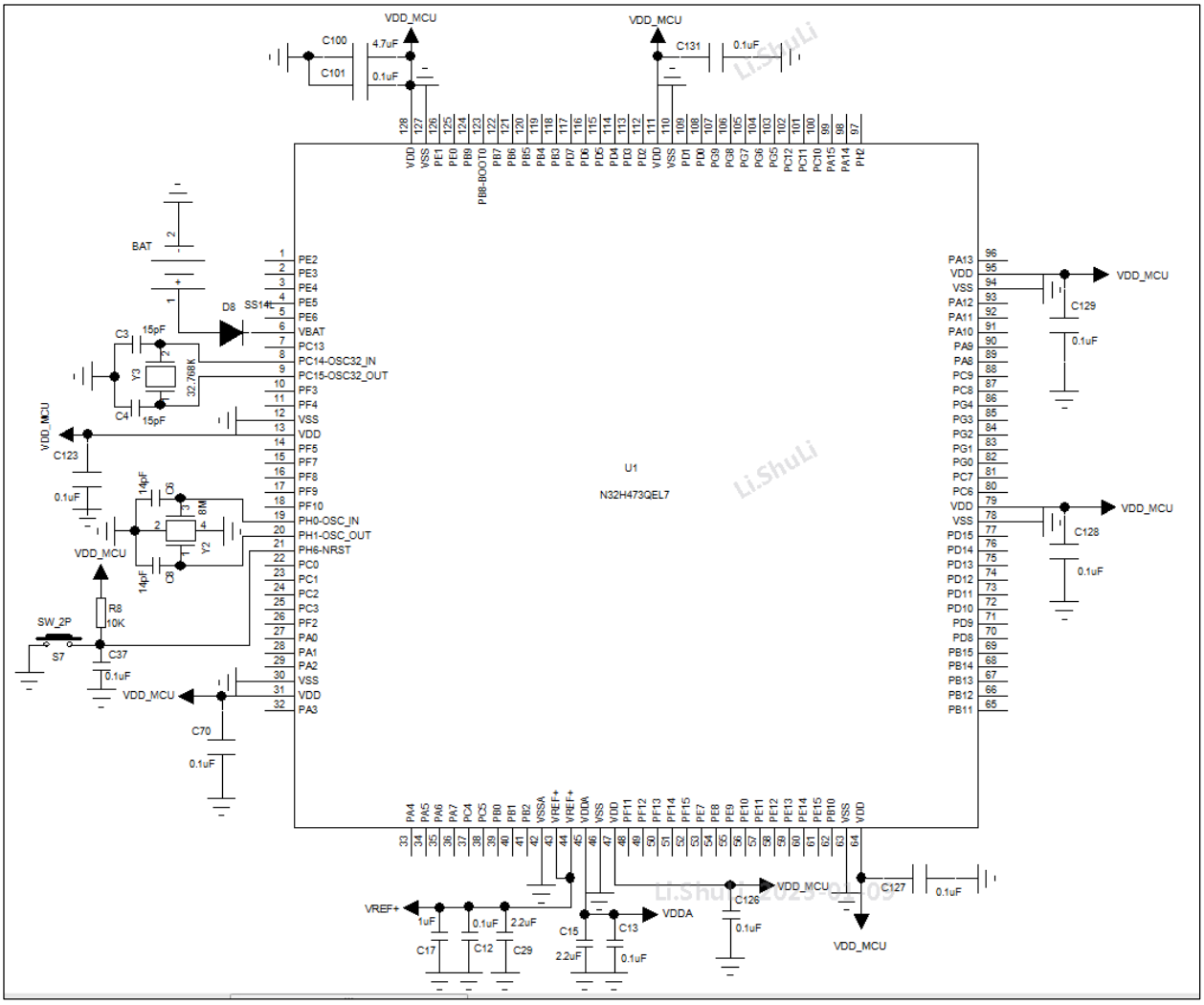

Figure 3-25 LQFP128 minimum package system reference design schematic diagram

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3.26 LQFP144-N32H482ZEL7

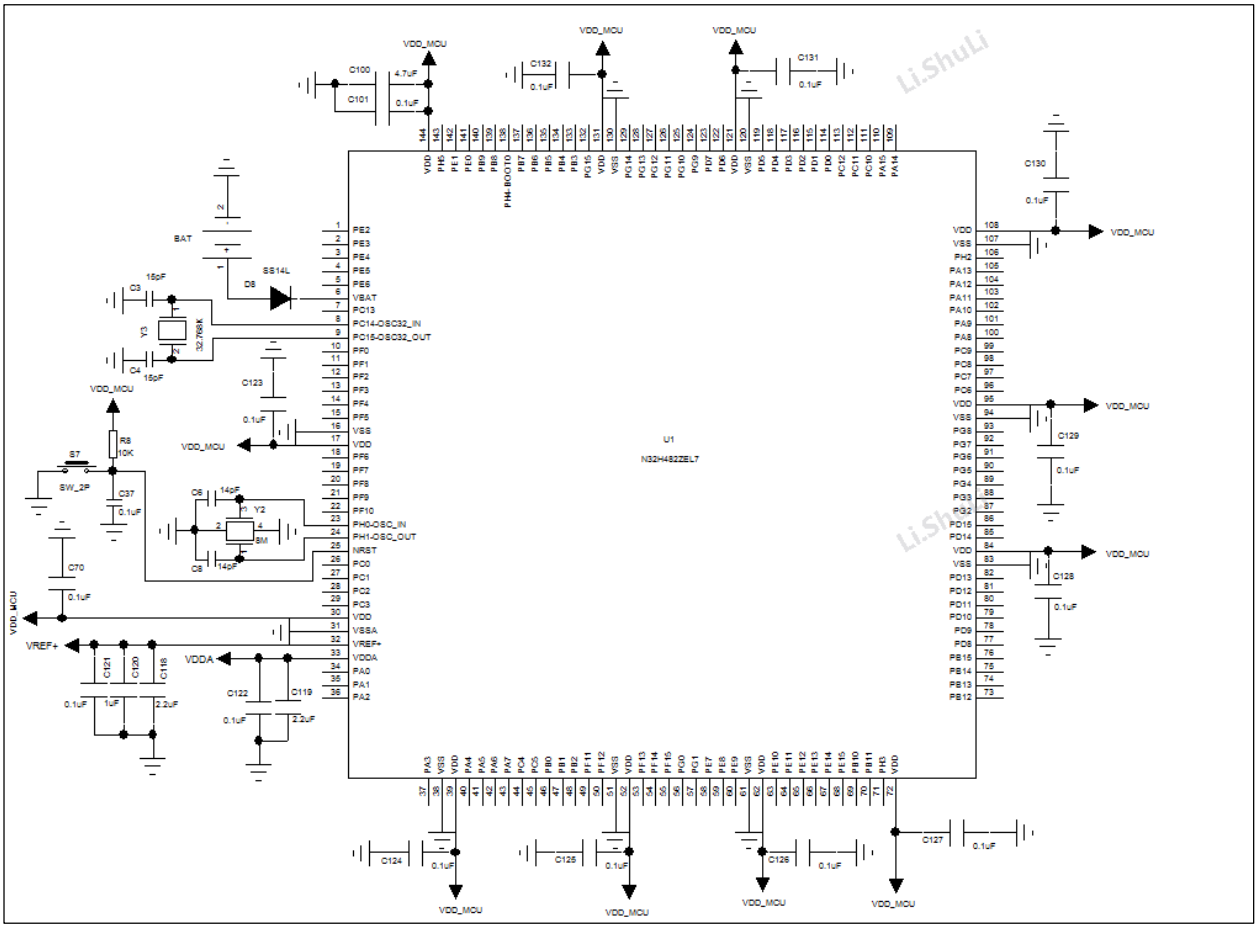

Figure 3-26 LQFP144 minimum package system reference design schematic diagram

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3.27 LQFP144-N32H487ZEL7

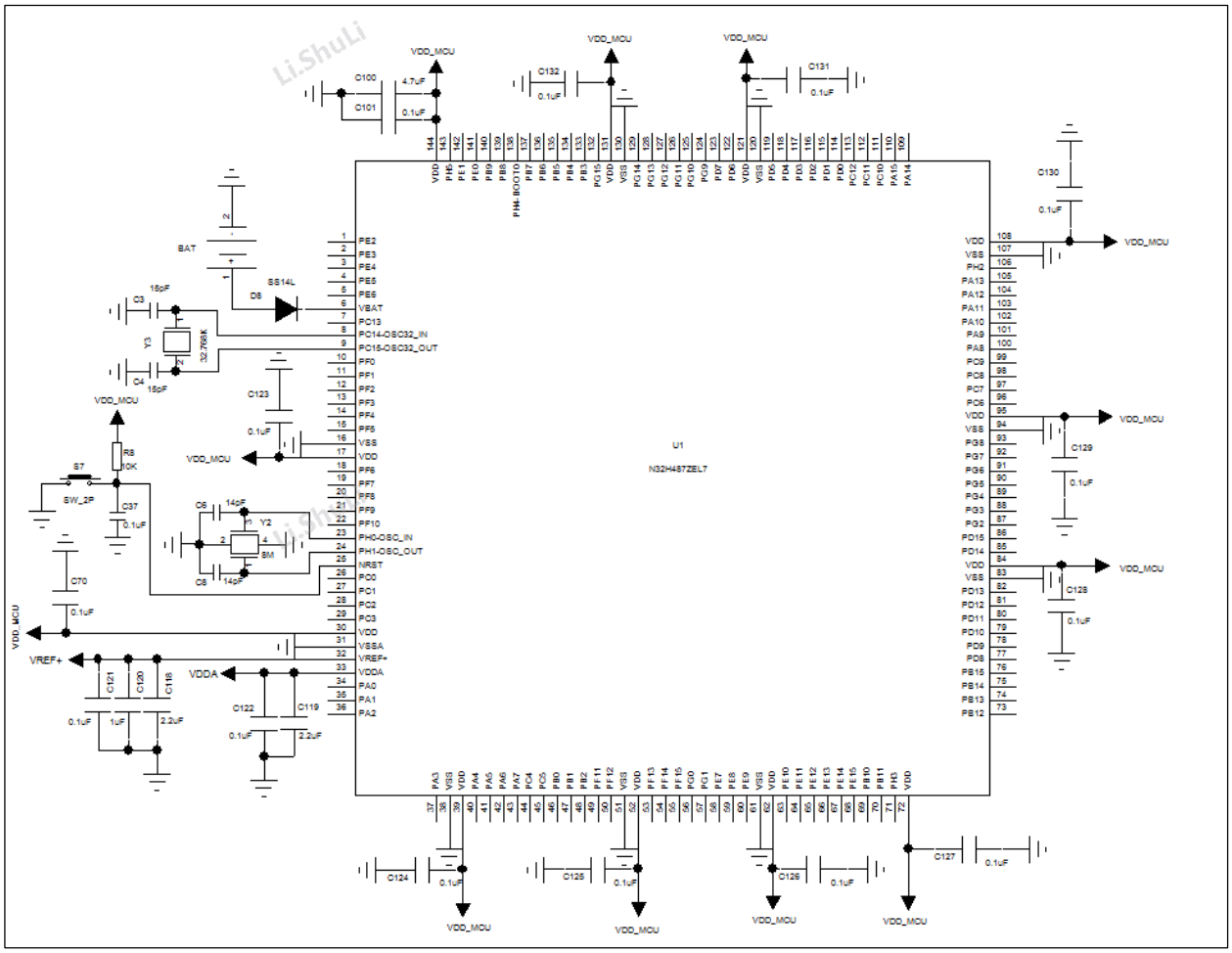

Figure 3-27 LQFP144 minimum package system reference design schematic diagram

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3.28 LQFP144-N32H488ZEL7

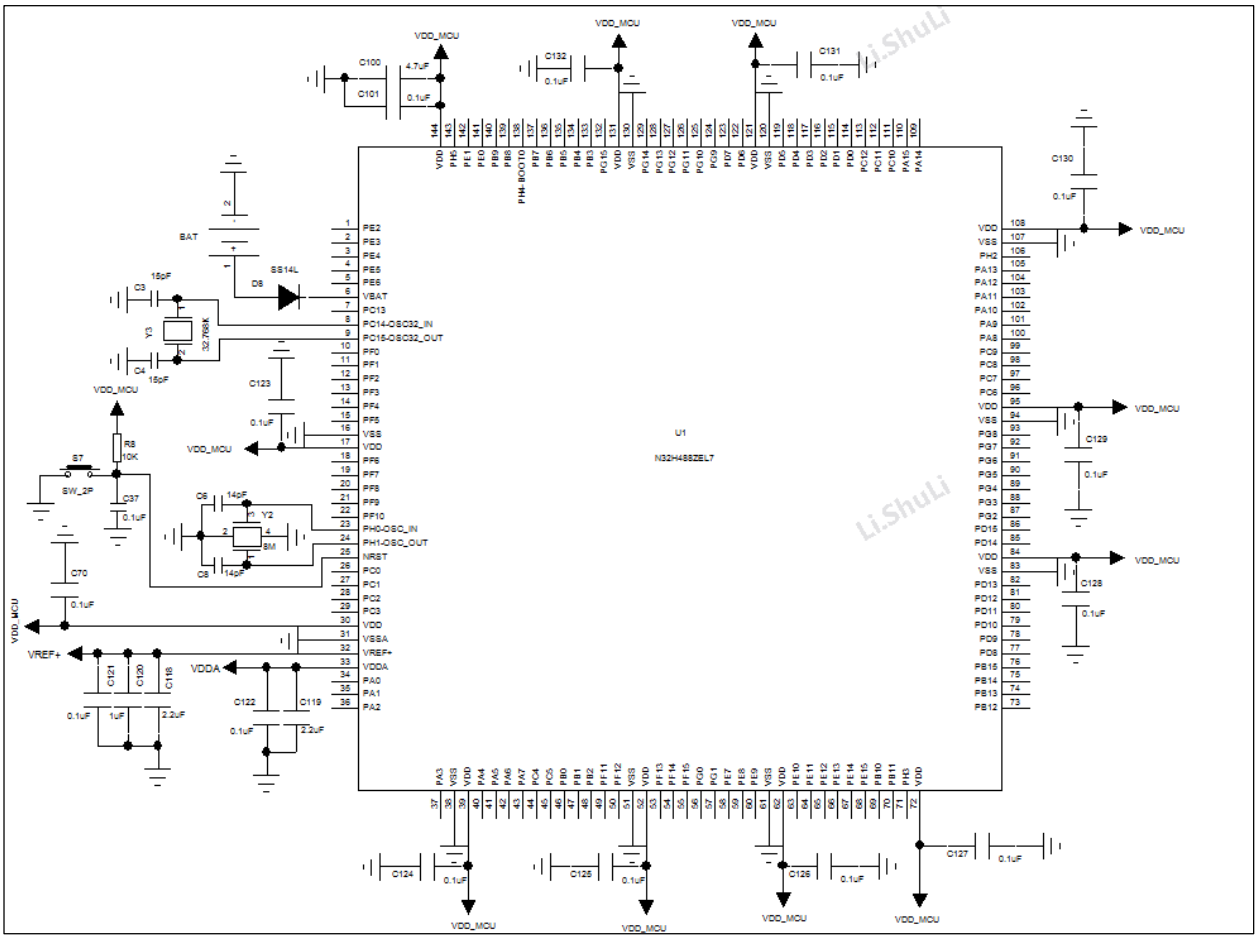

Figure 3-28 LQFP144 minimum package system reference design schematic diagram

The above is the minimum system reference design schematic diagram of different packages, which mainly reflects the design of power supply decoupling capacitor, clock, reset circuit, etc.;

Clock circuitry and battery backup depend on user design;

The chip supports internal high-speed and low-speed clocks for users to choose;

It is recommended that the analog power supply VDDA be powered by an external stable power supply. If it is directly connected to the VDD power supply, corresponding filtering needs to be done.

For N32H473/474/481/482/487/488 series chips:

When VERF+ uses the built-in reference source VREFBUF, it is recommended that a 0.1uF and a 1uF capacitor be placed nearby the VREF+ pin. When VERF+ is powered by an external source, it is recommended that a 0.1uF and a 2.2uF capacitor be placed nearby the VREF+ pin.

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4. PCB LAYOUT Reference

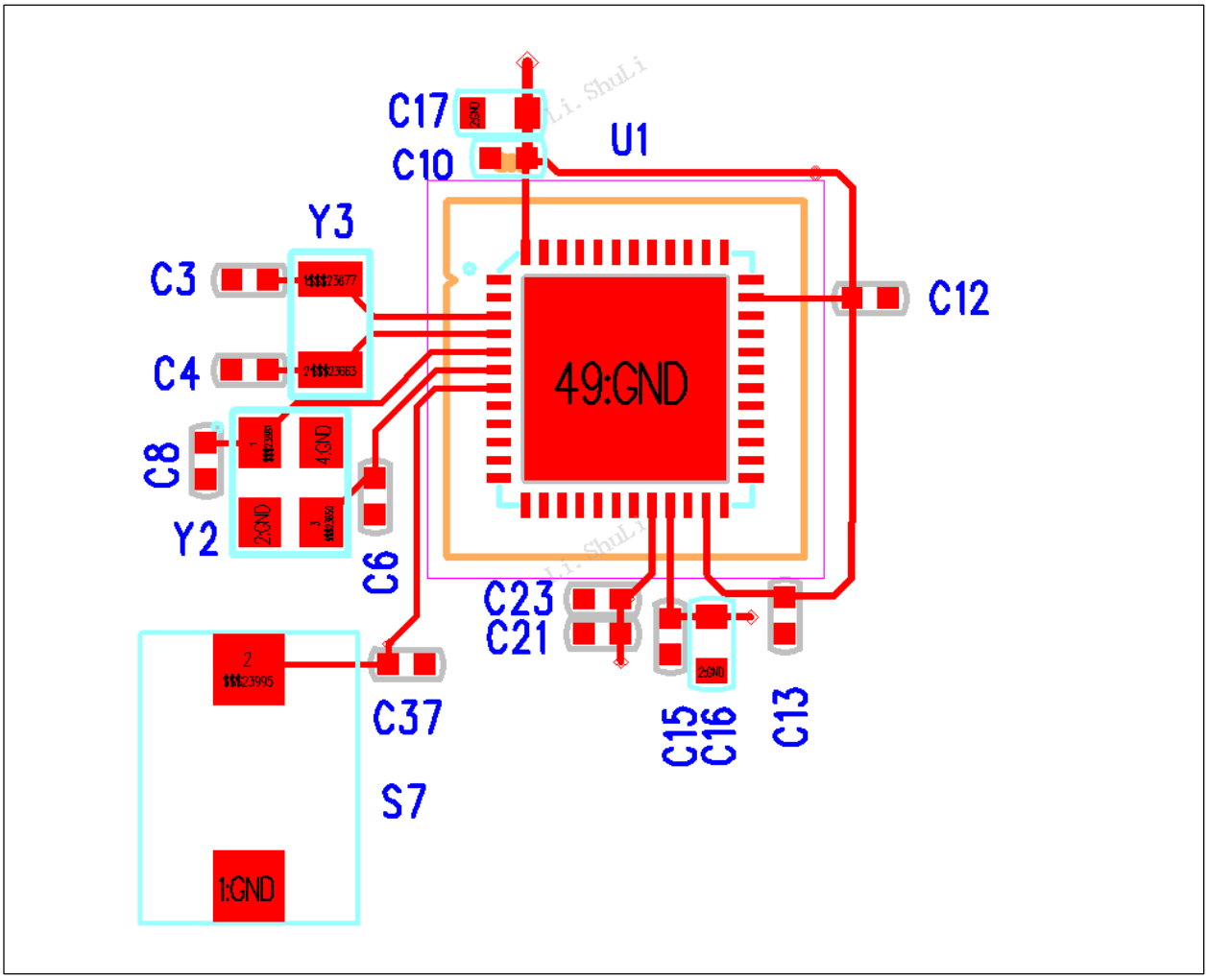

Figure 4-1 UQFN48 package PCB LAYOUT reference diagram

Note:

1、 When designing PCB LAYOUT, each power pin needs to be placed with a decoupling capacitor nearby;

2、 The external crystals and wiring of HSE and LSE should be covered with ground as much as possible. The area under the crystal near the crystal also needs to be paved. No signal lines can pass through to prevent the signal lines from interfering with the crystal signal;

3、 When HSE and LSE are used as crystal oscillators, the traces should not be too long to avoid antenna effects.

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5. Historical Versions

Version	Date	Remark
V1.0.0	2024-11-26	Create documentation

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